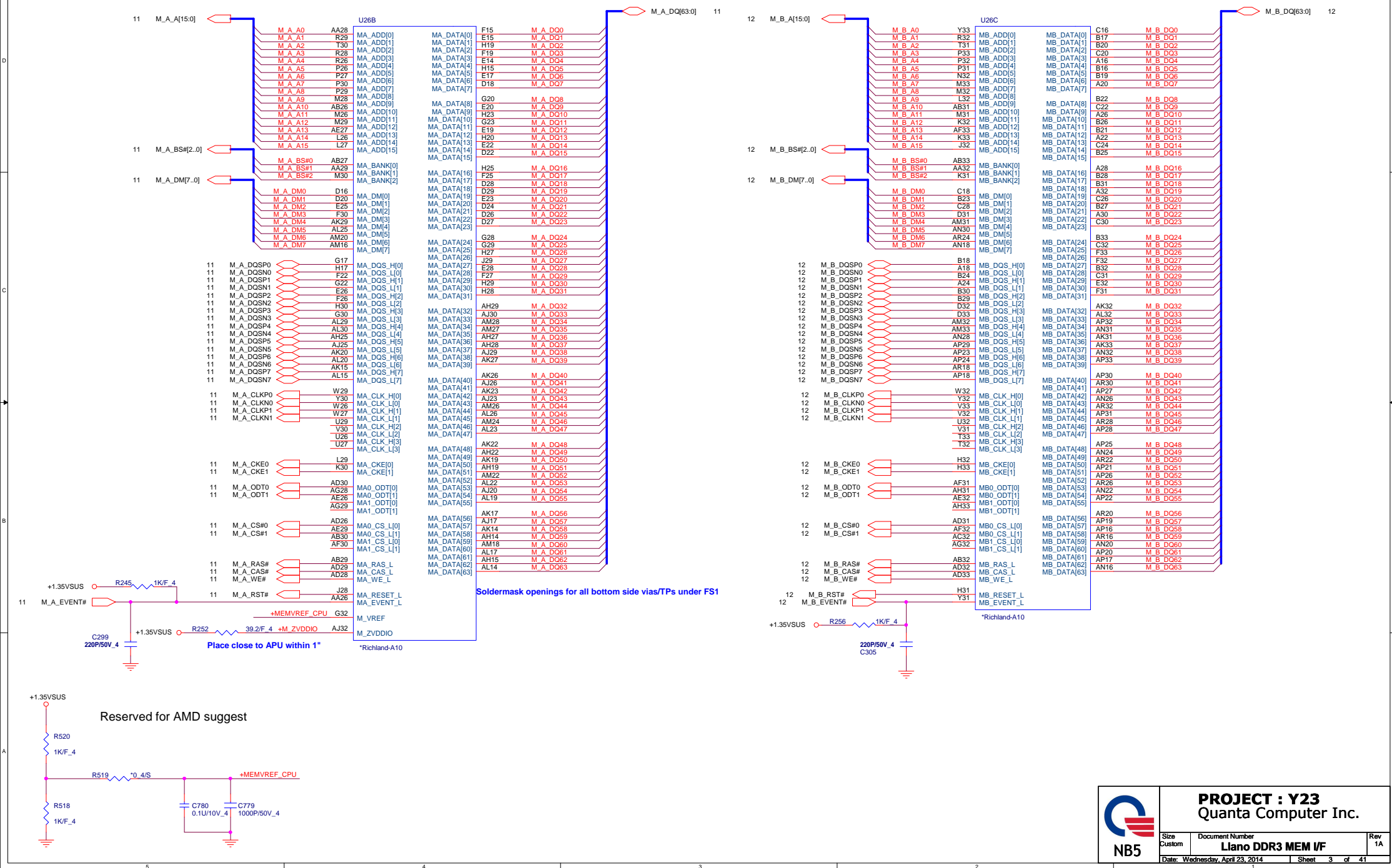
 NB5	PROJECT : Y23 Quanta Computer Inc.	
	Size Custom Liano PCIE/UMI/GPP	Document Number R
Date: Wednesday, April 23, 2014		Sheet 2 of 41



Display port power 1.5V min 1.2v max : 1.65v

11/27:for eDP dual channel

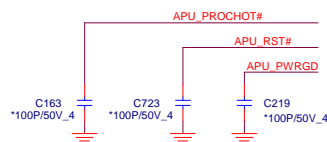
4/19 HDMI change to DP2 for Comal.

**DP2 output to
HDMI connector**

note -HDMI P&N can not swap

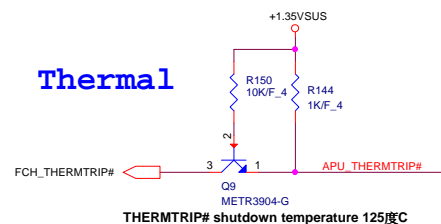
Note: CLK_APU_HCLKP/N is 100MHZ SSC

Note: CLK_DP_NSSCP/N is 100MHZ non-S

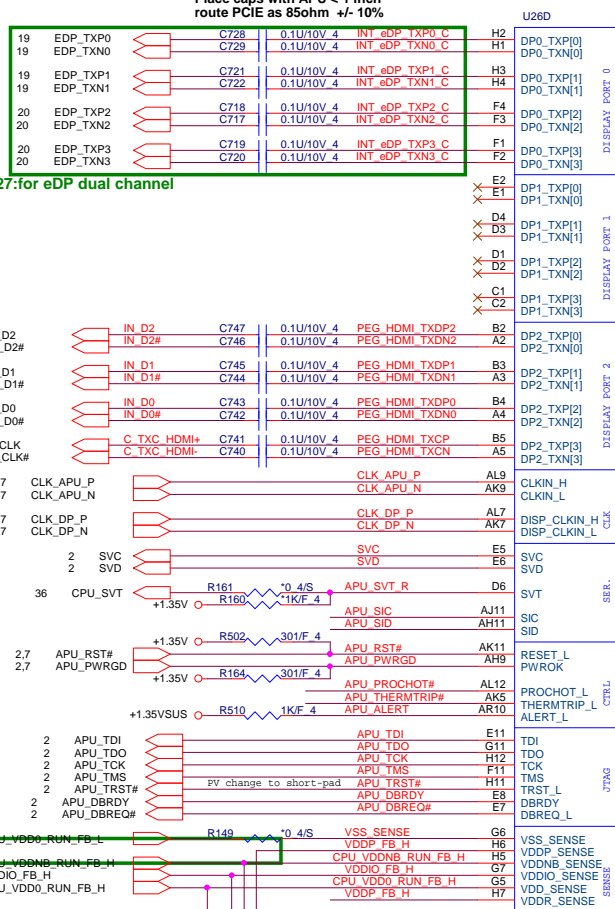
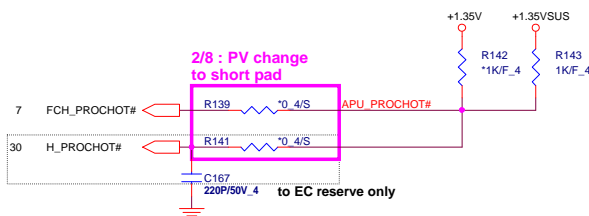


11/27:remove for Power no use³

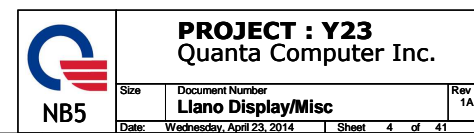
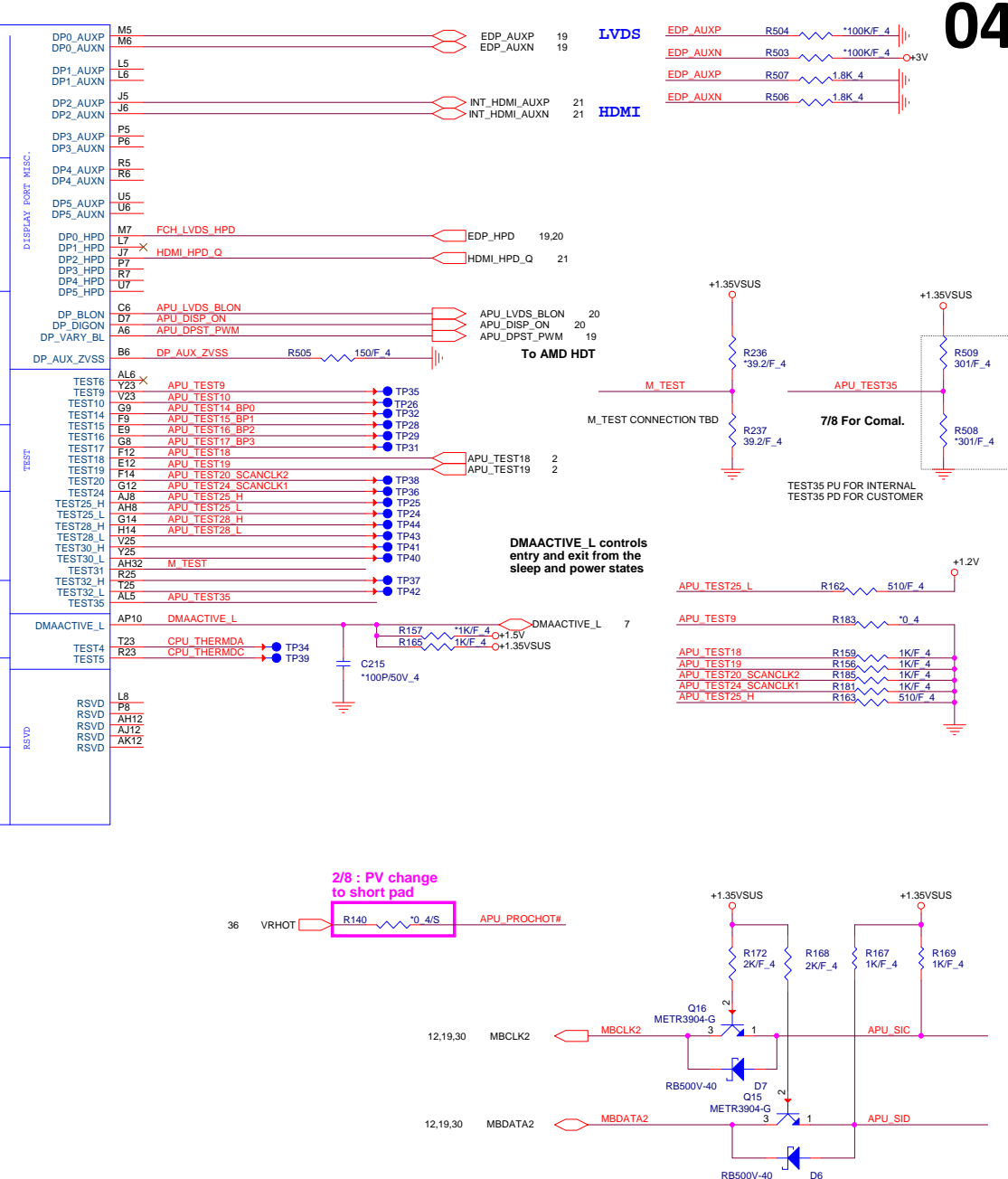
Thermal



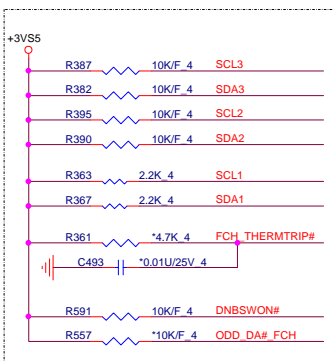
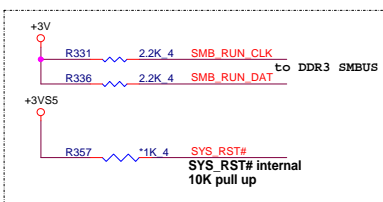
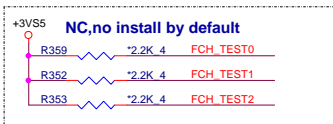
**4/19 For Comal,
close to APU.**



*Richland-A10



VDDR

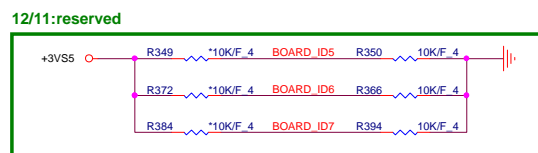


GEVENT0# internal pull Hi 8.2K to +3V
GEVENT1# internal pull Hi 8.2K to +3V
GEVENT23# internal pull Hi 8.2K to +3V
GEVENT5# internal pull Hi 8.2K to +3V5S
PCIE_WAKE# no need to pull Hi resistor from check list
SYS_RST# internal 10K pull up

CLK_REQ2# internal pull Hi 8.2K to +3V
CLK_REQ3# internal pull Hi 8.2K to +3V
CLK_REQ4# internal pull Hi 8.2K to +3V

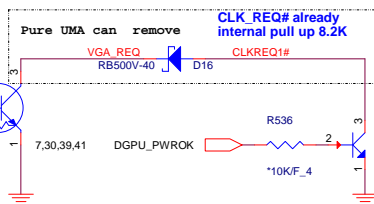
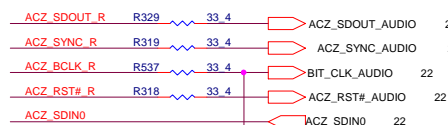
This pin is used to power down VGA DAC regulators when CRT no connected

GEVENT16# internal pull Hi 8.2K to +3V5S
GEVENT15# internal pull Hi 8.2K to +3V5S



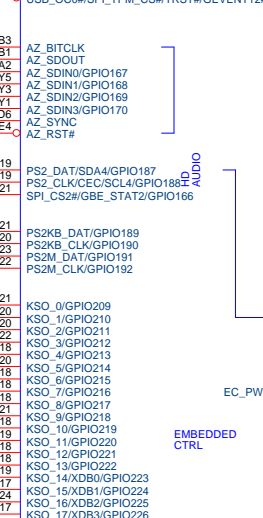
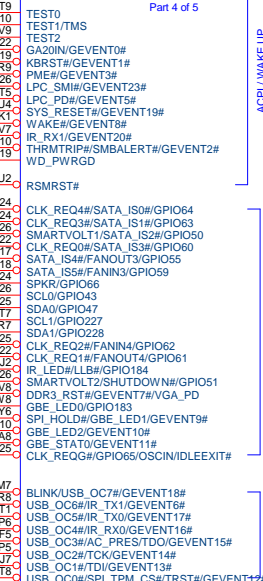
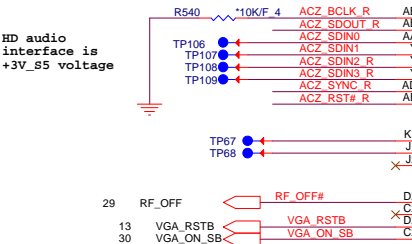
Board ID [5:7]	Definition
000	Reserve (Default = 000)

To Azalia

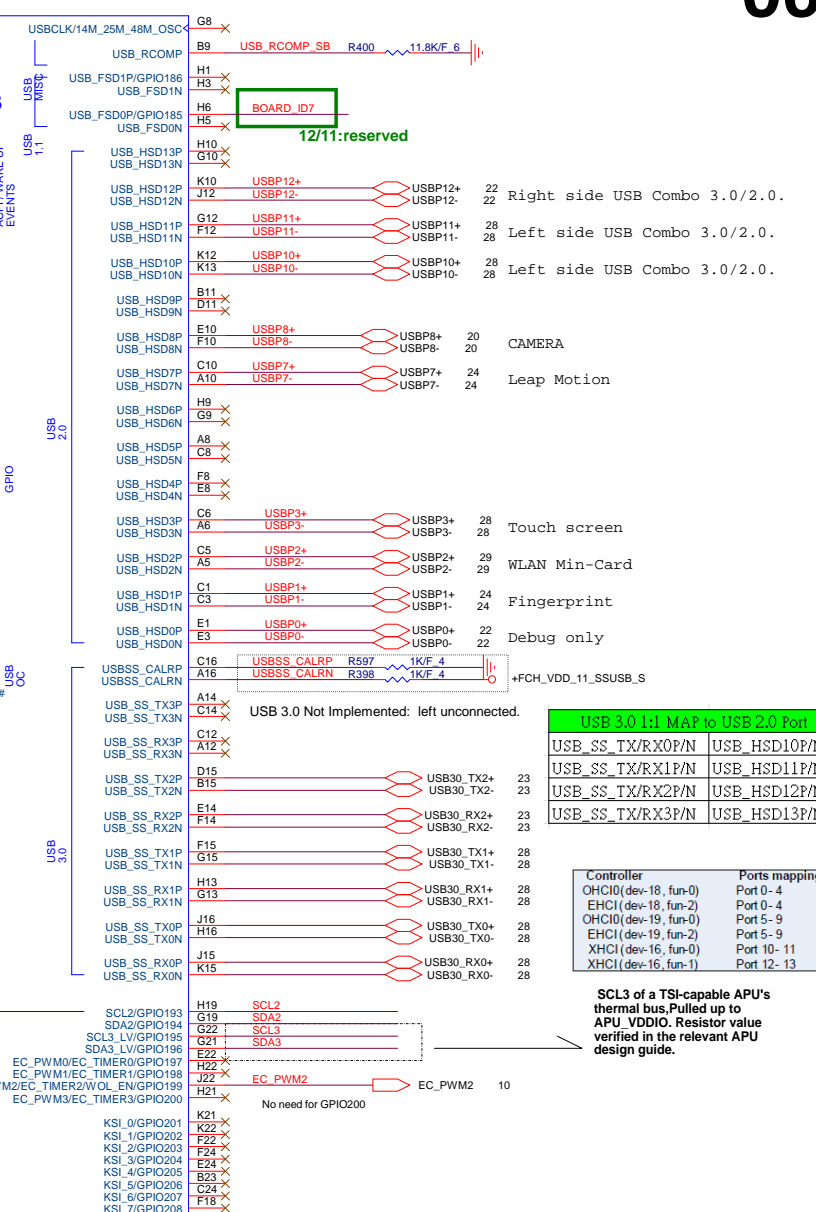


For Zero ODD

HD audio interface is +3V_S5 voltage



EMBEDDED CTRL

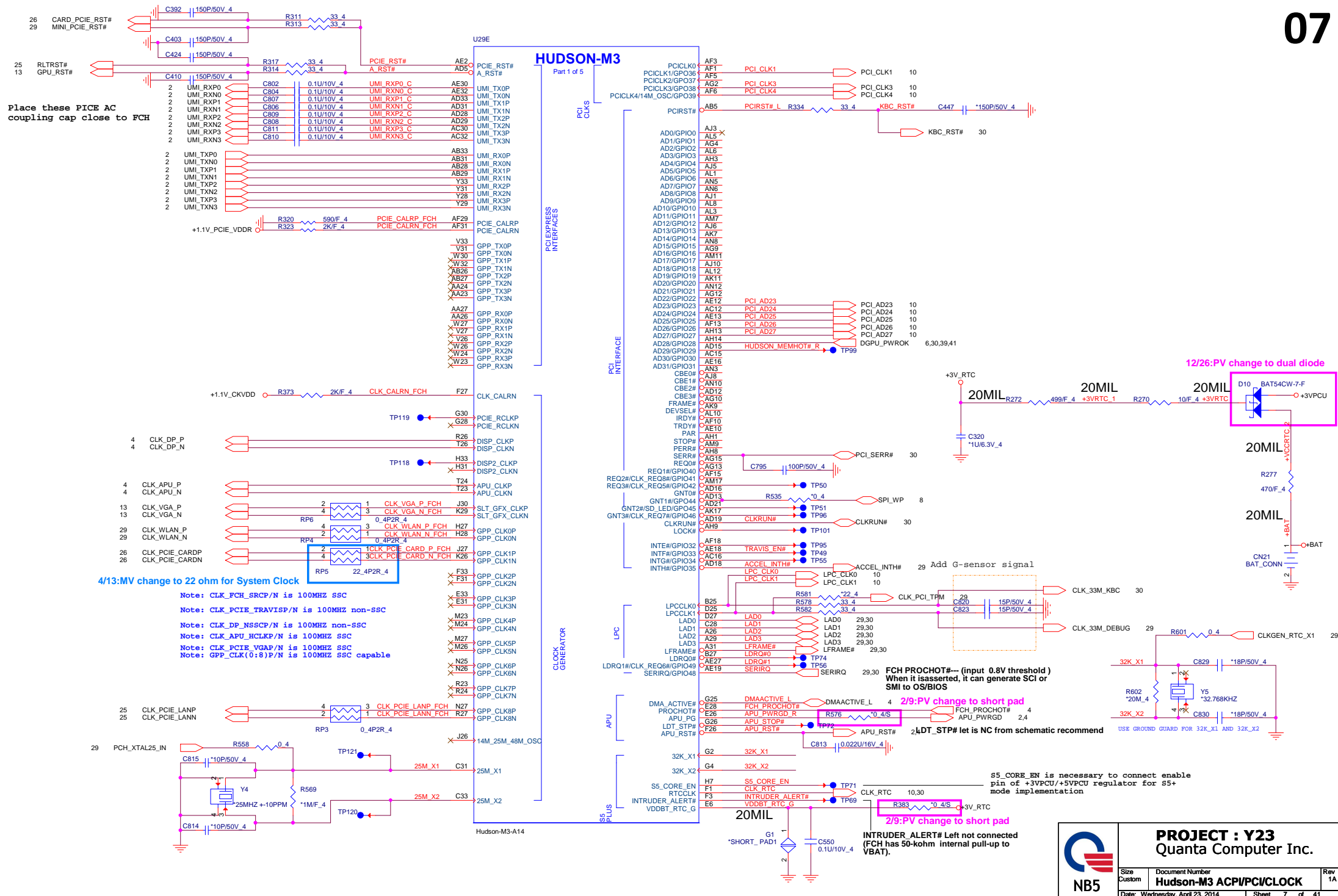


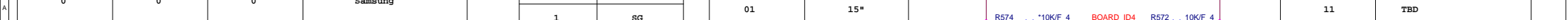
USB 3.0 1:1 MAP to USB 2.0 Port

USB_SS_TX/RX0P/N	USB_HSD10P/N
USB_SS_TX/RX1P/N	USB_HSD11P/N
USB_SS_TX/RX2P/N	USB_HSD12P/N
USB_SS_TX/RX3P/N	USB_HSD13P/N

Controller	Ports mapping
OHCI0 (dev-18, fun-0)	Port 0-4
EHCI (dev-18, fun-2)	Port 0-4
OHCI0 (dev-19, fun-0)	Port 5-9
EHCI (dev-19, fun-2)	Port 5-9
XHCI (dev-16, fun-1)	Port 10-11
XHCI (dev-16, fun-1)	Port 12-13

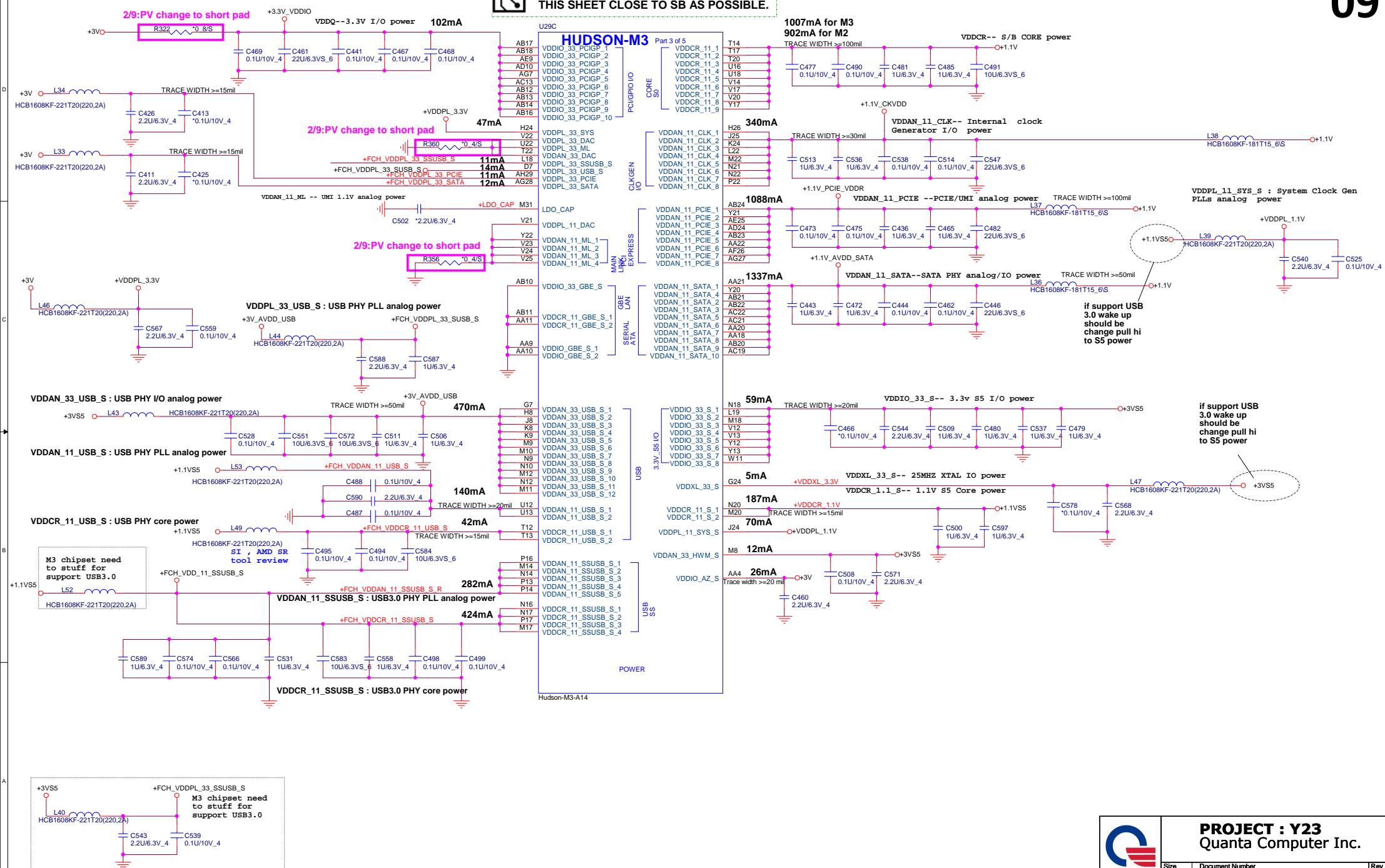
SCL3 of a TSI-capable APU's thermal bus. Pulled up to APU_VDDIO. Resistor value verified in the relevant APU design guide.





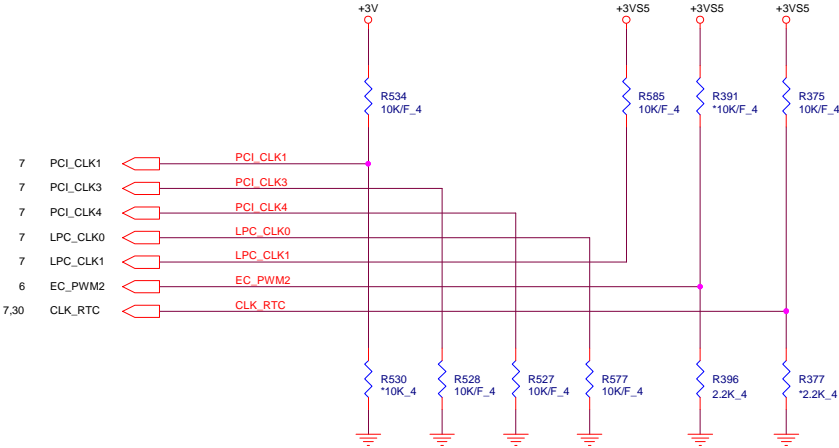


PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.



STRAPS PINS

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.



REQUIRED STRAPS

		PCI_CLK1		PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	CLK_RTC
PULL HIGH		ALLOW PCIE Gen2 DEFAULT		USE DEBUG STRAP	non Fusion CLOCK MODE	AMD internal EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE ENABLED DEFAULT
PULL LOW		FORCE PCIE Gen1		IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED	SPI ROM DEFAULT	S5 PLUS MODE DISABLED

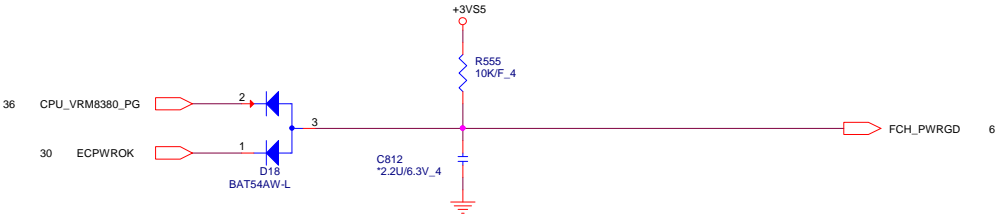
DEBUG STRAPS

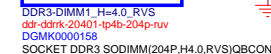
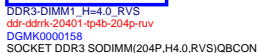
FCH has 15K Internal Pull Up for PCI_AD[27:23]



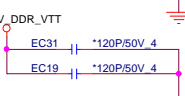
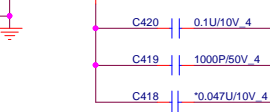
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

FCH_PWRGD



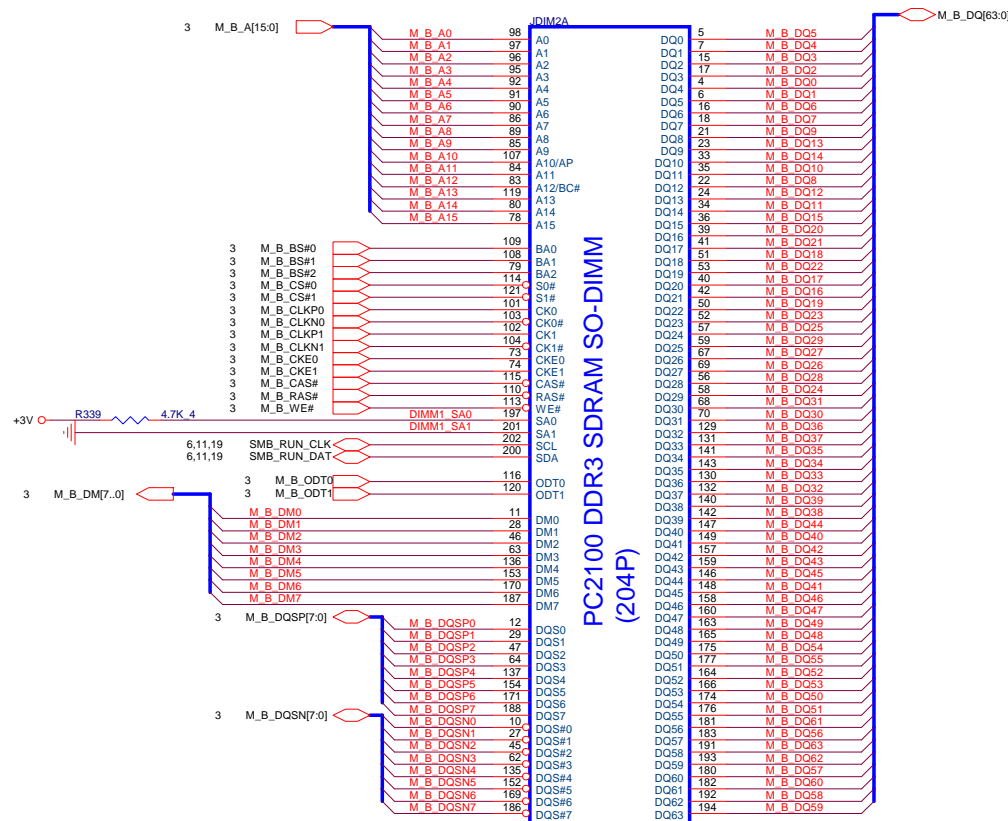


Place these Caps near So-Dimm0.



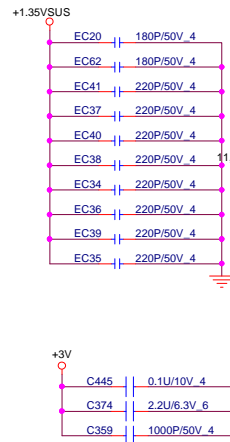
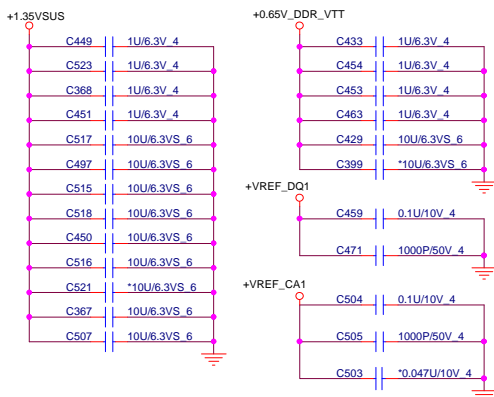
PROJECT : Y23
Quanta Computer Inc.

Size Custom	Document Number System Memory 1/2 (4H)	Rev 1A
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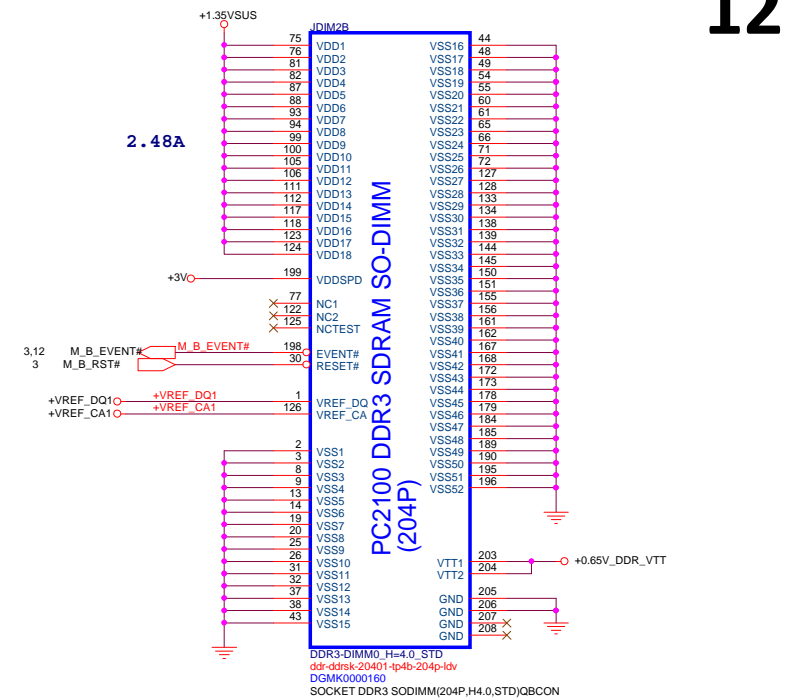
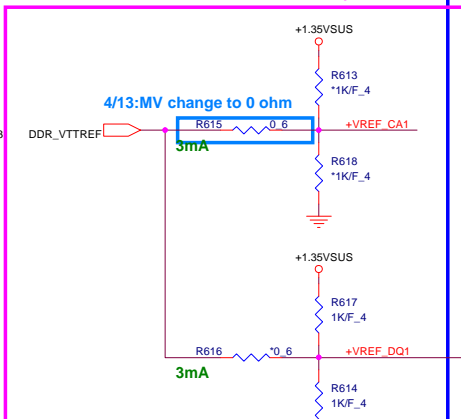


DDR3-DIMM0_H=4.0_STD
ddr-ddrsk-20401-tp4b-204p-ldv
DGMK0000160
SOCKET DDR3 SODIMM(204P,H4.0,STD)QBCON

Place these Caps near So-Dimm1.



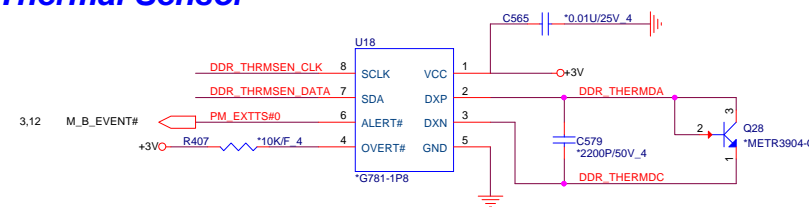
2/7 : PV modify



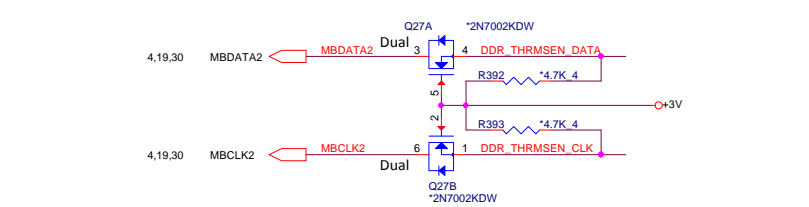
DDR3-DIMM0_H=4.0_STD
ddr-ddrsk-20401-tp4b-204p-ldv
DGMK0000160
SOCKET DDR3 SODIMM(204P,H4.0,STD)QBCON

Local Thermal Sensor

DDR3 Thermal Sensor



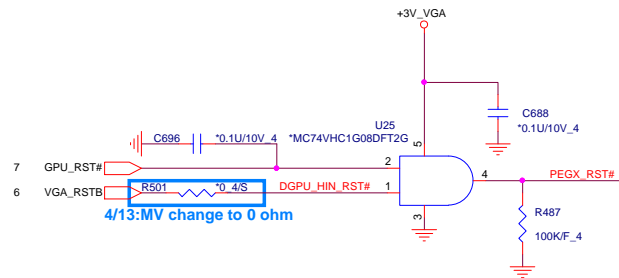
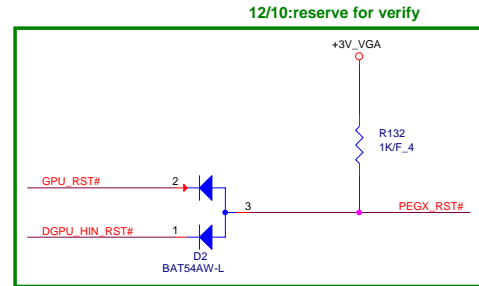
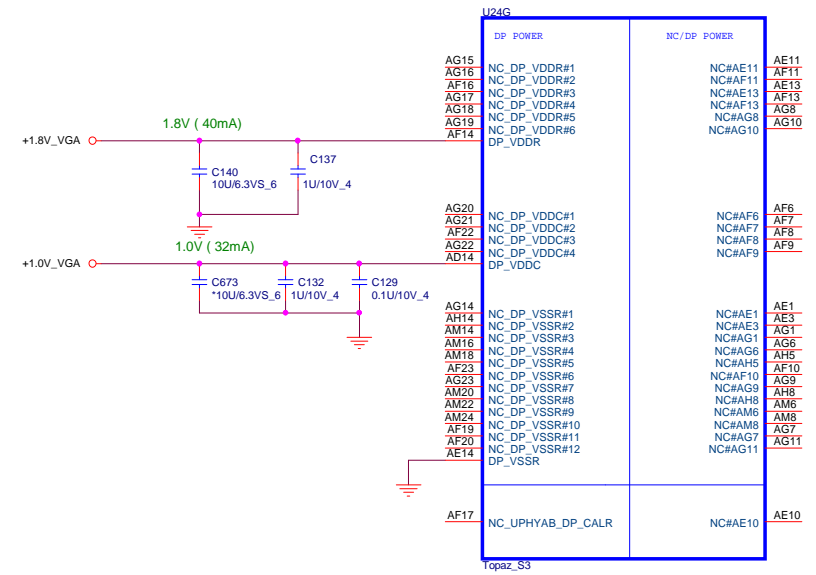
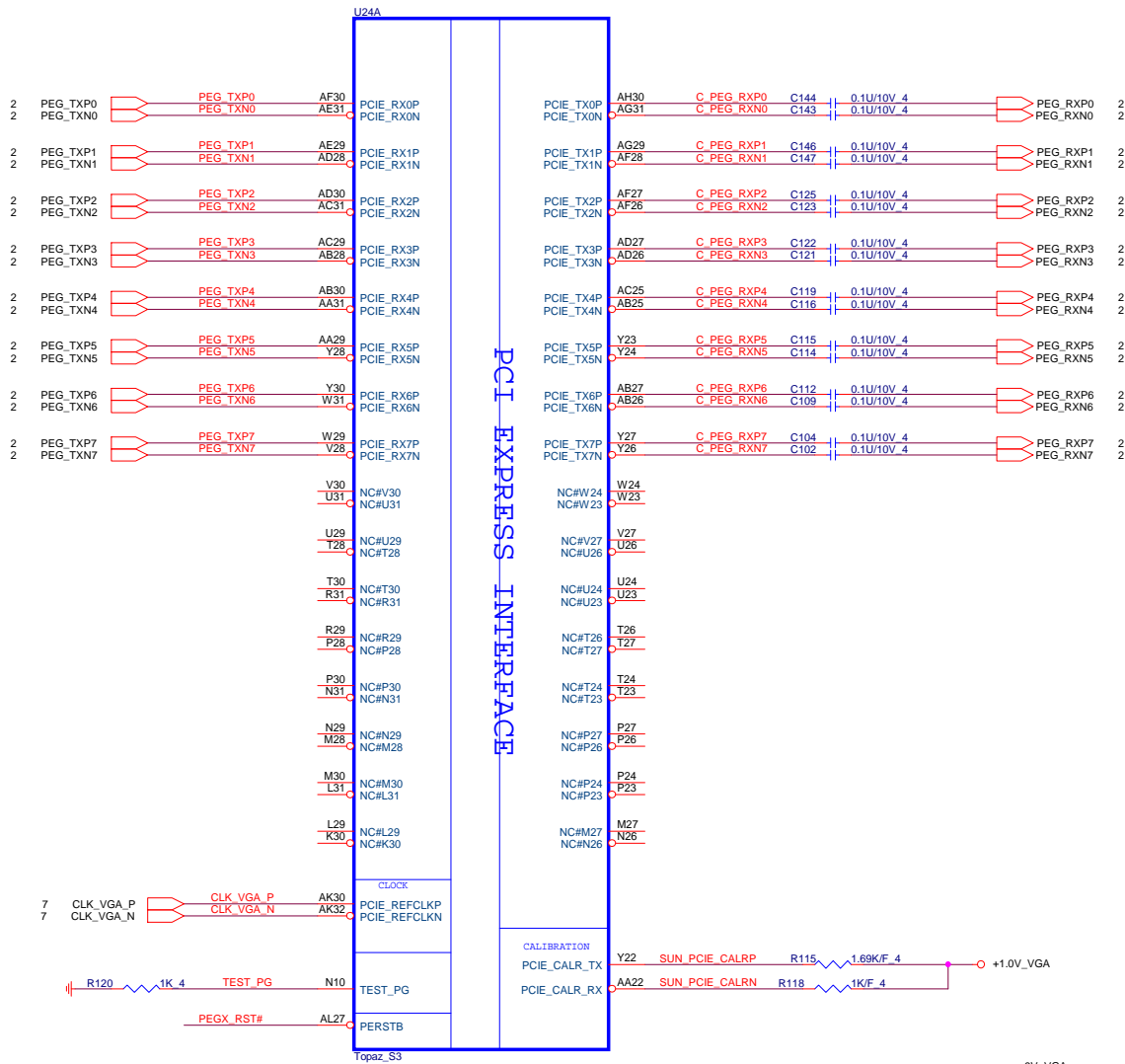
If use internal thermal IC, C9007 use 0ohm.



Main:AL000781039
2nd:AL001412005
Main:AL001412003
2nd:AL000431014

G781-1P8(9Ah)
EMC1412-2-ACZL-TR(9Ah)
EMC1412-1-ACZL-TR(98h)
TMP431ADGKR(98h)

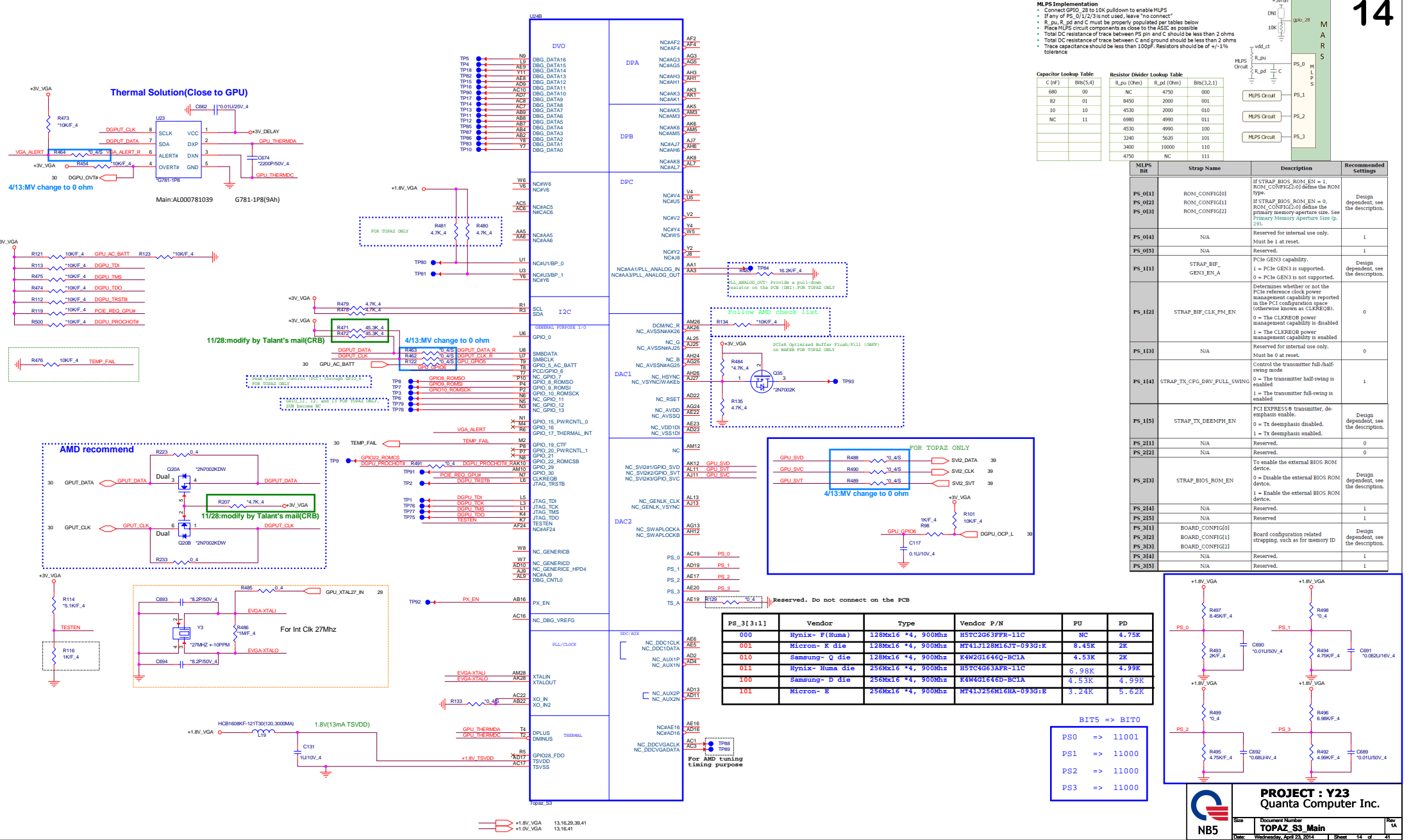
PROJECT : Y23		
Quanta Computer Inc.		
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14,16,30,41 +3V_VGA

14,16,29,39,41 +1.8V_VGA

16,41 +1.0V_VGA



MLPS Implementation

- Connect GPIO_28 to 10K pull-down to enable MLPS
- If any of PS_0/1/2/3 is not used, leave "no connect"
- R_{pu}, R_{pd} and C must be properly populated per table below
- Place MLPS circuit components as close to the ASIC as possible
- Total DC resistance of trace between PS pin and C should be less than 2 ohms
- Total DC resistance of trace between C and ground should be less than 2 ohms
- Trace capacitance should be less than 100pF. Resistors should be of +/-1% tolerance

Capacitor Lookup Table

C (pF)	Bin(3,4)	R _{pu} (Ohm)	R _{pd} (Ohm)	Bin(3,2,1)
680	00	NC	4750	000
82	01	8450	2000	001
10	10	4530	2000	010
NC	11	6980	4990	011
		4530	4990	100
		3240	5620	101
		3400	10000	110
		4750	NC	111

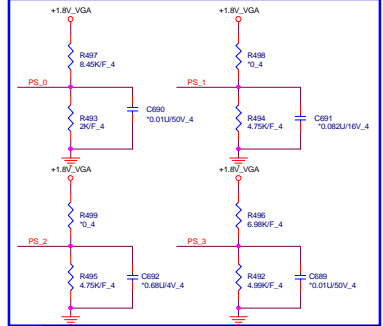
Resistor Divider Lookup Table

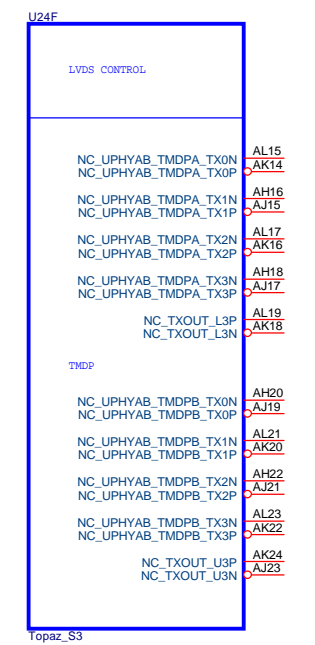
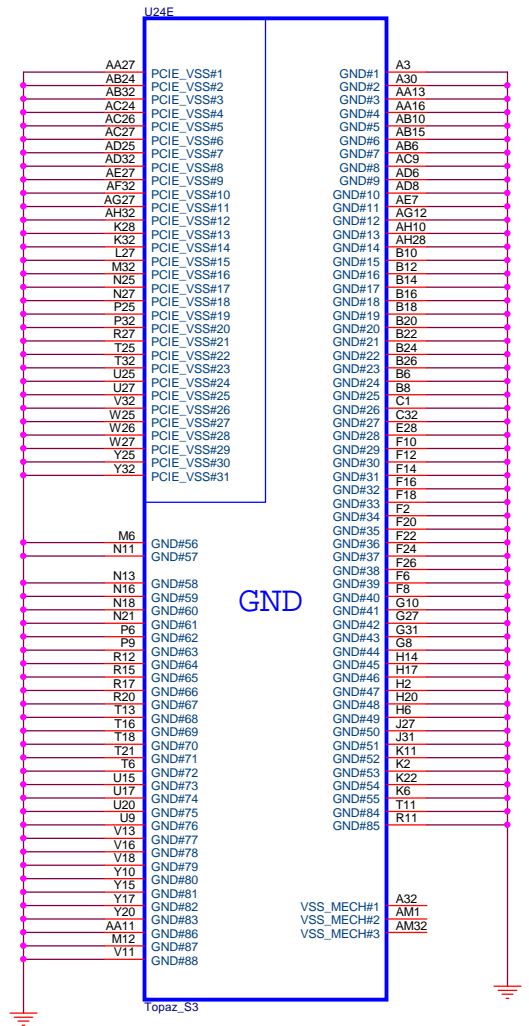
R _{pu} (Ohm)	R _{pd} (Ohm)	Bin(3,2,1)
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

MLPS Circuit diagrams for PS_0, PS_1, PS_2, PS_3.

MLPS Bit	Strap Name	Description	Recommended Settings
PS_011	ROM_CONFIG[0]	If STRAP_BIOS_ROM_EN = 1, ROM_CONFIG[0] defines the ROM type.	Design dependent, see the description.
PS_012	ROM_CONFIG[1]	If STRAP_BIOS_ROM_EN = 0, ROM_CONFIG[1] defines the primary memory aperture size. See Primary Memory Aperture Size (p. 29).	
PS_013	ROM_CONFIG[2]		
PS_041	N/A	Reserved for internal use only. Must be 1 at reset.	1
PS_015	N/A	Reserved.	1
PS_111	STRAP_BIF_GEN3_EN_A	PCIe GEN3 capability. 1 = PCIe GEN3 is supported. 0 = PCIe GEN3 is not supported.	Design dependent, see the description.
PS_112	STRAP_BIF_CLK_PM_EN	Determines whether or not the PCIe reference clock power management capability is reported in the PCI configuration space (otherwise known as CLKREQ#). 1 = The CLKREQ# power management capability is disabled. 0 = The CLKREQ# power management capability is enabled.	0
PS_113	N/A	Reserved for internal use only. Must be 0 at reset.	0
PS_114	STRAP_TX_CFG_DRV_FULL_SWING	Control the transmitter full-half-swing mode. 0 = The transmitter half-swing is enabled. 1 = The transmitter full-swing is enabled.	1
PS_115	STRAP_TX_DEENPH_EN	PCI EXPRESS transmitter, de-emphasis enable. 0 = Tx deemphas disabled. 1 = Tx deemphas enabled.	Design dependent, see the description.
PS_211	N/A	Reserved.	0
PS_212	N/A	Reserved.	0
PS_213	STRAP_BIOS_ROM_EN	To enable the external BIOS ROM device. 0 = Disable the external BIOS ROM device. 1 = Enable the external BIOS ROM device.	Design dependent, see the description.
PS_214	N/A	Reserved.	1
PS_215	N/A	Reserved.	1
PS_311	BOARD_CONFIG[0]	Board configuration related strapping, such as for memory ID	Design dependent, see the description.
PS_312	BOARD_CONFIG[1]		
PS_313	BOARD_CONFIG[2]		
PS_314	N/A	Reserved.	1
PS_315	N/A	Reserved.	1

PS_3[3:1]	Vendor	Type	Vendor P/N	PU	PD
000	Hynix- F(Huma)	128Mx16 *4, 900Mhz	H5TC2G63FPR-11C	NC	4.75K
001	Micron- K die	128Mx16 *4, 900Mhz	MT41J128M16JT-093G:R	8.45K	2K
010	Samsung- Q die	128Mx16 *4, 900Mhz	K4W2G1646Q-BC1A	4.53K	2K
011	Hynix- Huma die	256Mx16 *4, 900Mhz	H5TC4G63AFR-11C	6.98K	4.99K
100	Samsung- D die	256Mx16 *4, 900Mhz	K4W4G1646Q-BC1A	4.53K	4.99K
101	Micron- E	256Mx16 *4, 900Mhz	MT41J256M16HA-093B:E	3.24K	5.62K





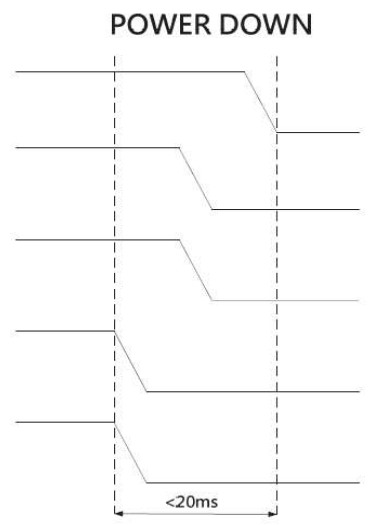
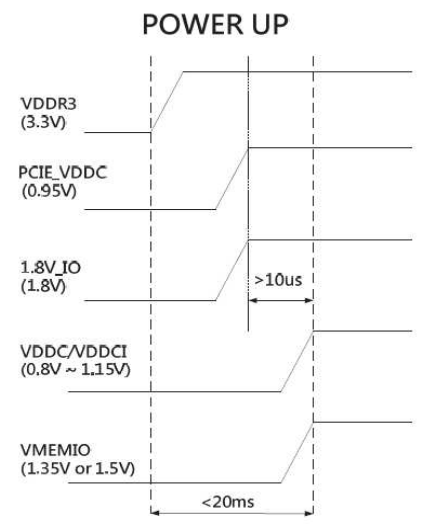
CONFIGURATION STRAPS-- SEE EACH DATABOOK FOR STRAP DETAILS ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET			RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1 = INSTALL 3K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
RSVD	GPIO2	RESERVED	0
RSVD	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS (Removed on Seymour/Whistler)	0
RSVD	H2SYNC	RESERVED	0
AUD[1]	HSYNC	SEE DATABOOK FOR DETAIL	0
AUD[0]	VSYNC	SEE DATABOOK FOR DETAIL	0
RSVD	GENERICC	RESERVED	0

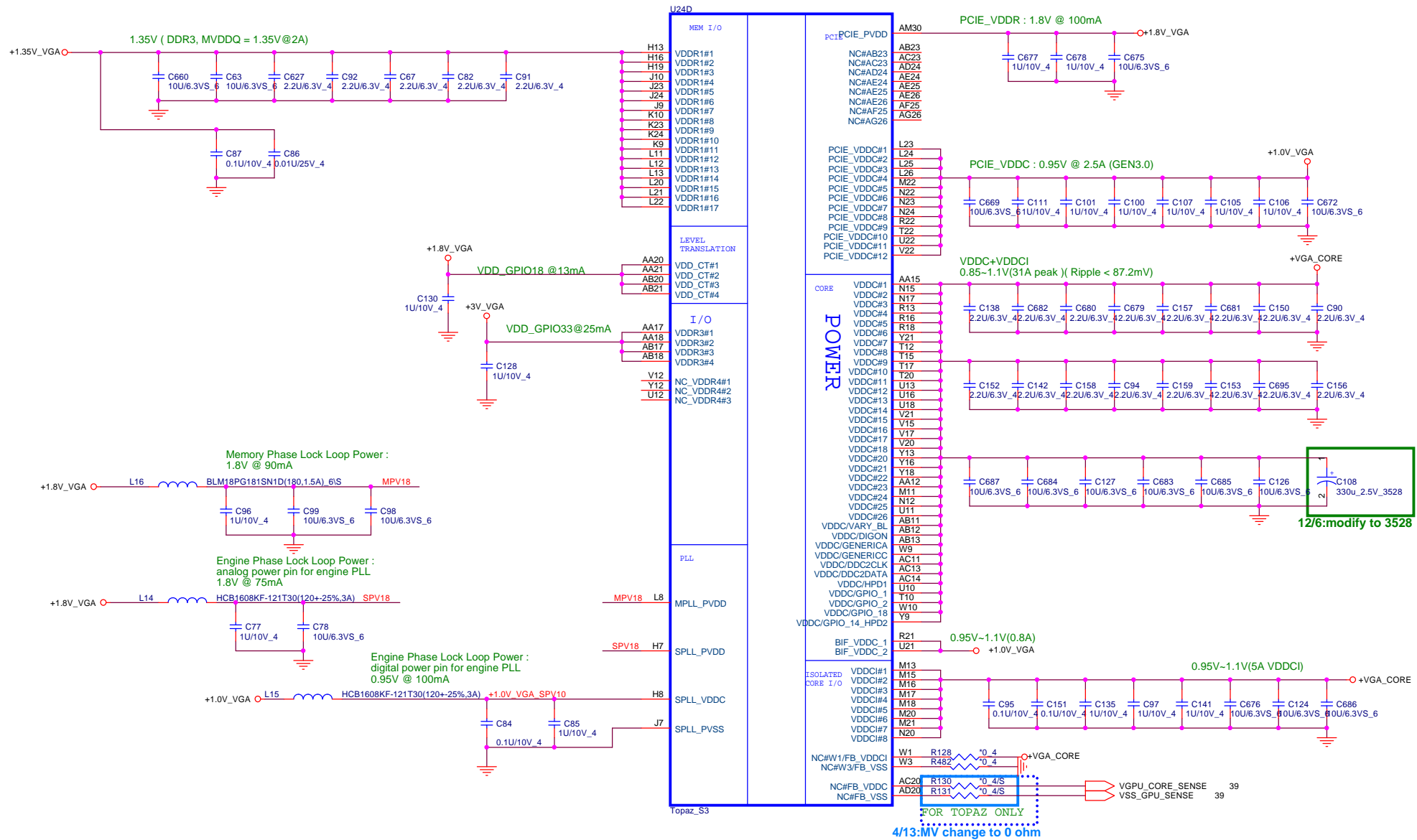
NOTE1: AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOS ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET.

GPIO21 H2SYNC GENERICC GPIO8 GPIO2

POWER UP / POWER DOWN SEQUENCE



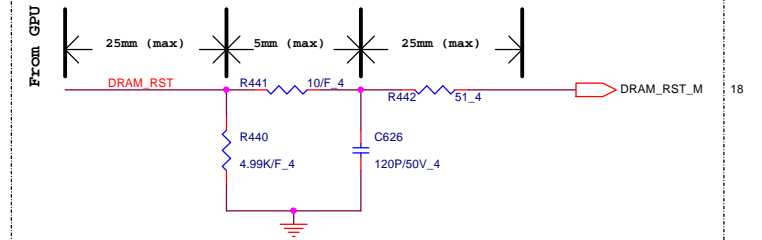
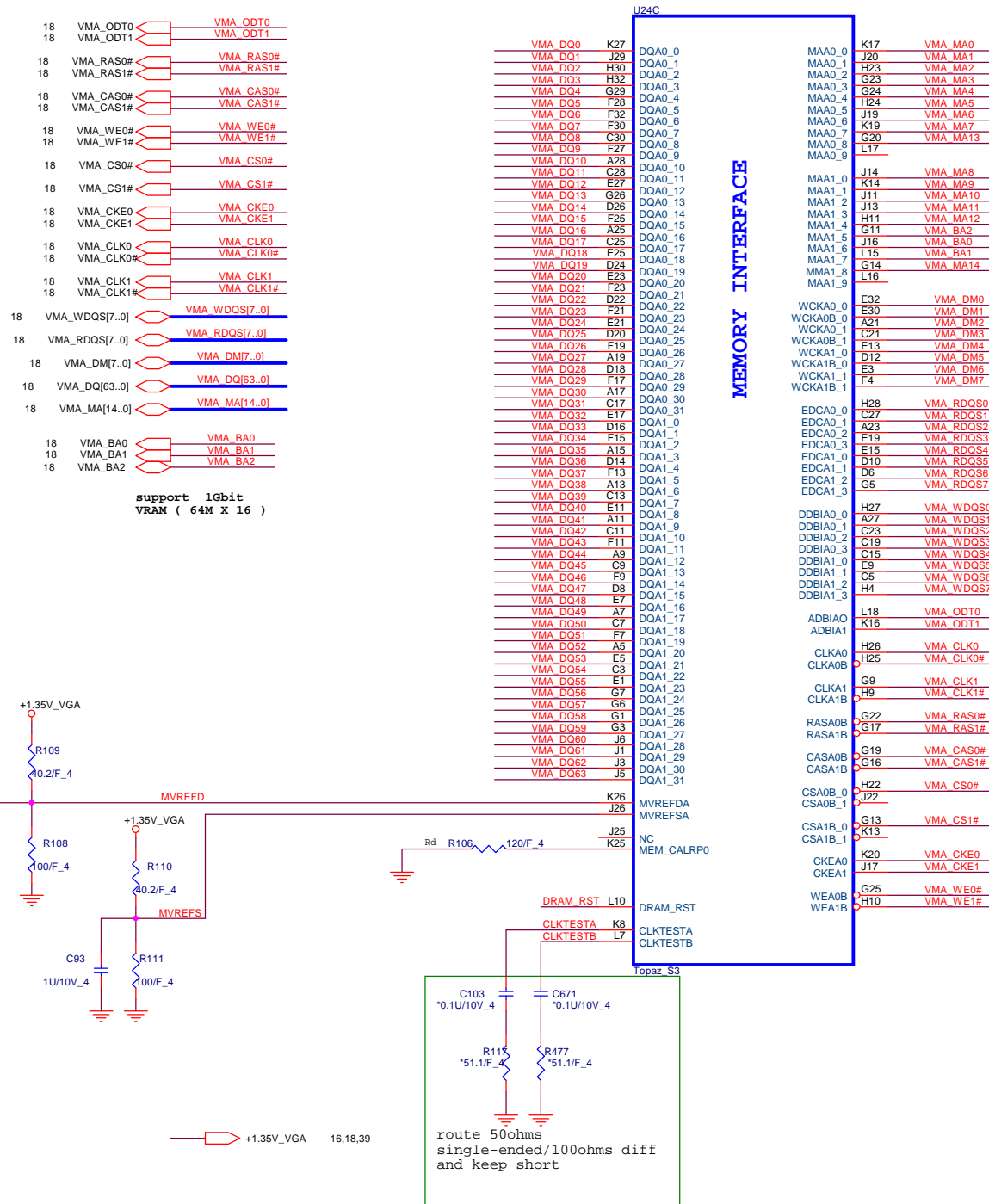


+1.35V_VGA	17,18,39
+1.8V_VGA	13,14,29,39,41
+1.0V_VGA	13,41
+VGA_CORE	39,40



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	TOPAZ S3 Power	1A
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Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2

This basic topology should be used for DRAM_RST for DDR3/GDDR5. These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.

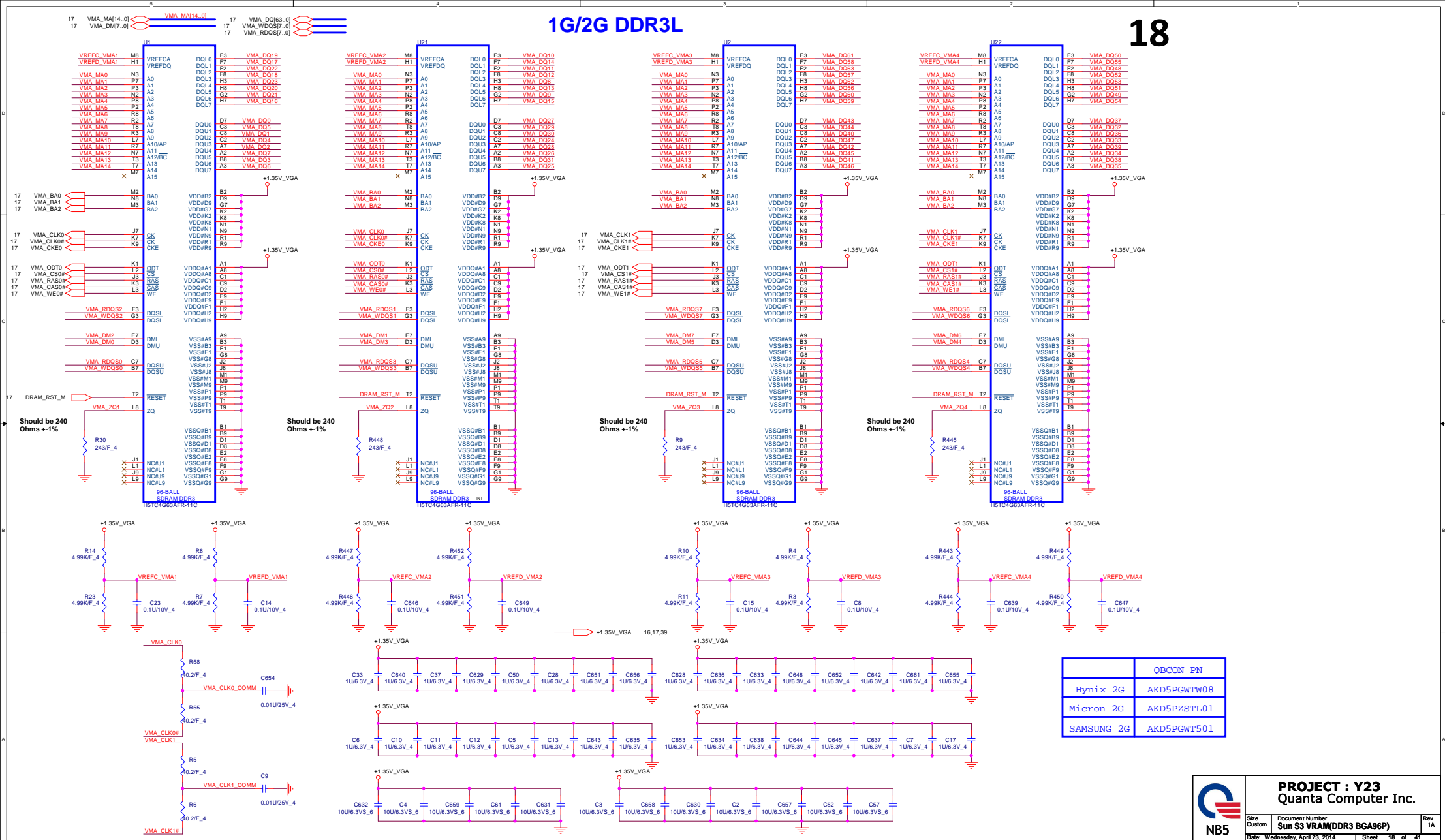


PROJECT : Y23
Quanta Computer Inc.

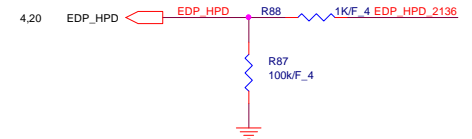
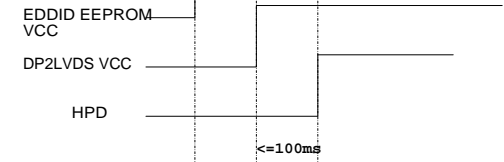
Size	Document Number	Rev
	TPOAZ_S3_MEM_Interface	1A
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1G/2G DDR3L

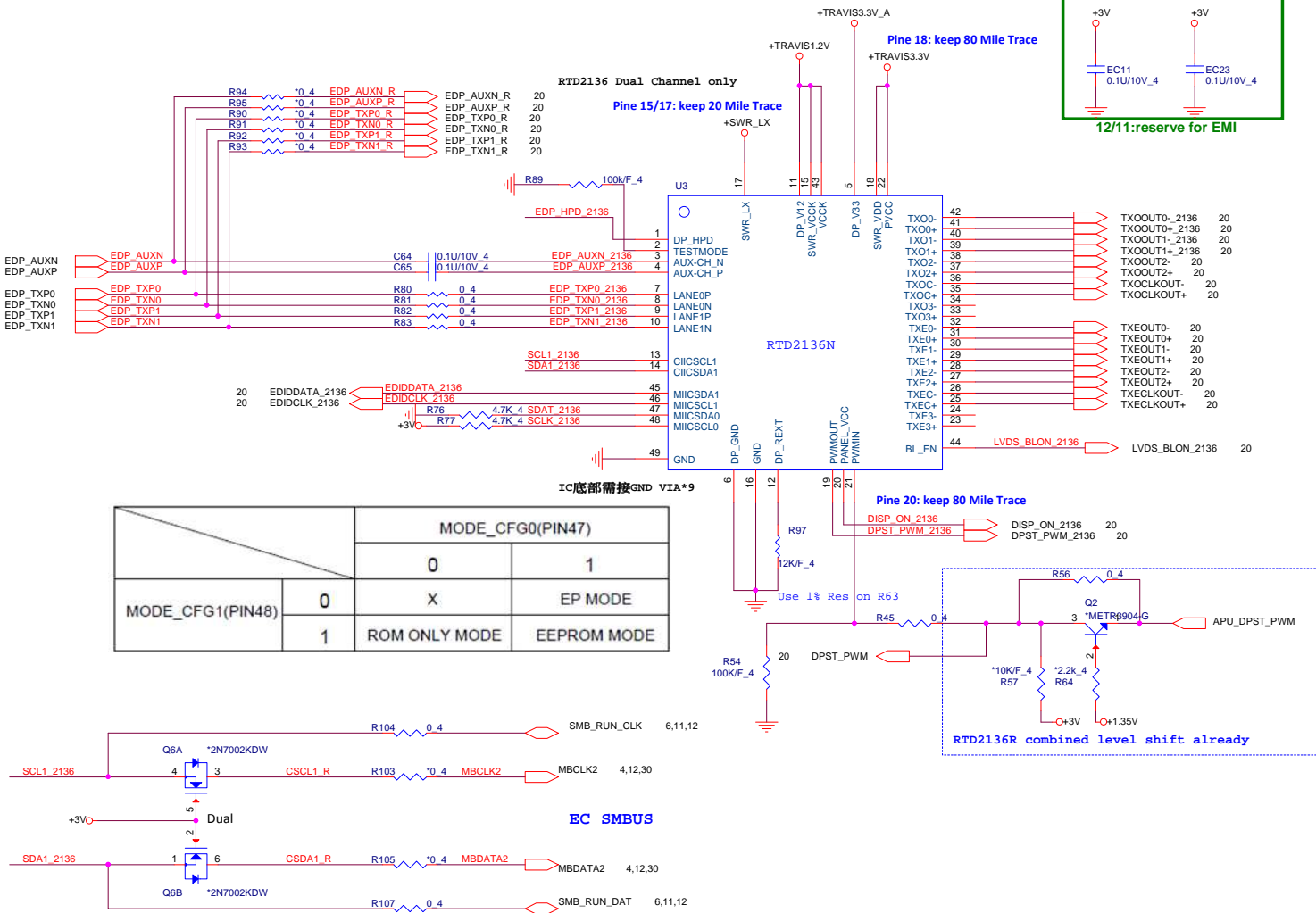
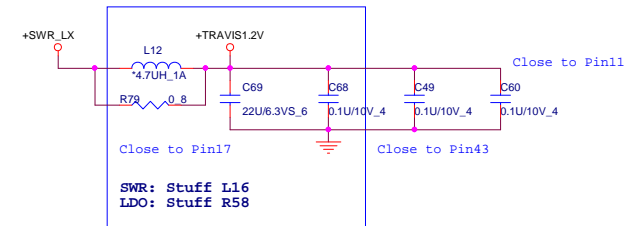
18



RTD2136S Power Up Sequence

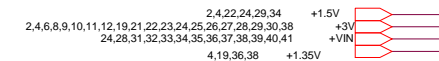
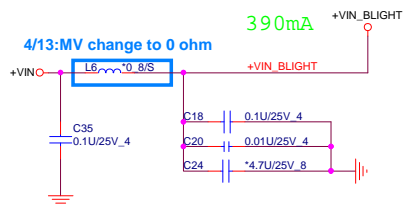
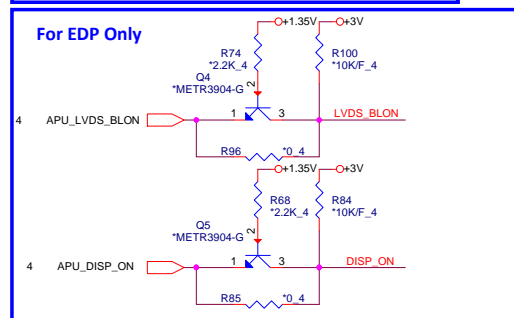
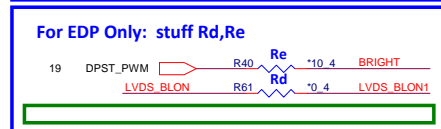
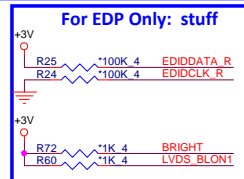
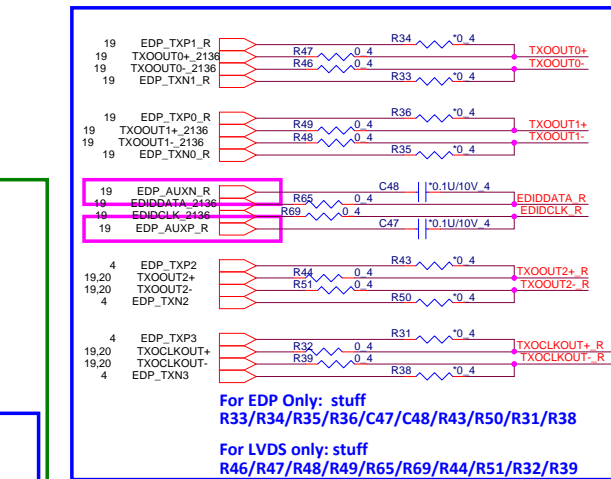
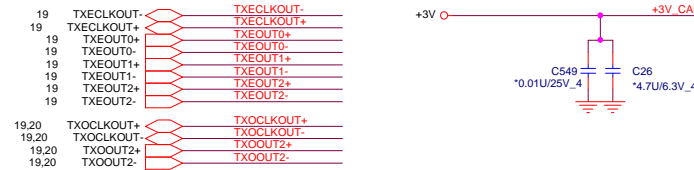


L69: need use CV-4709MN00 for Vendor suggestion
2nd CV-4708MN03



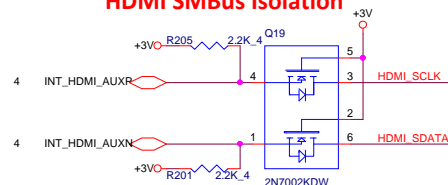
2,4,6,8,9,10,11,12,20,21,22,23,24,25,26,27,28,29,30,38
4.20,36,38 +1.35V
+3V
2.4,22,24,29,34 +1.5V

20



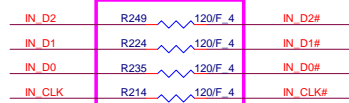
HDMI Conn.

HDMI SMBus Isolation

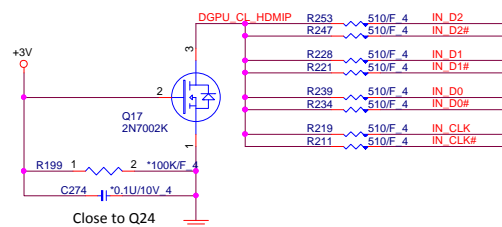


Close to HDMI connector

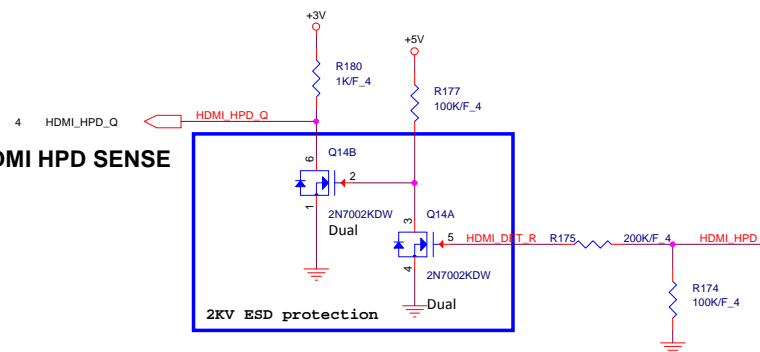
2/9:modify for HDMI fail



Check list recommend 604 ohm

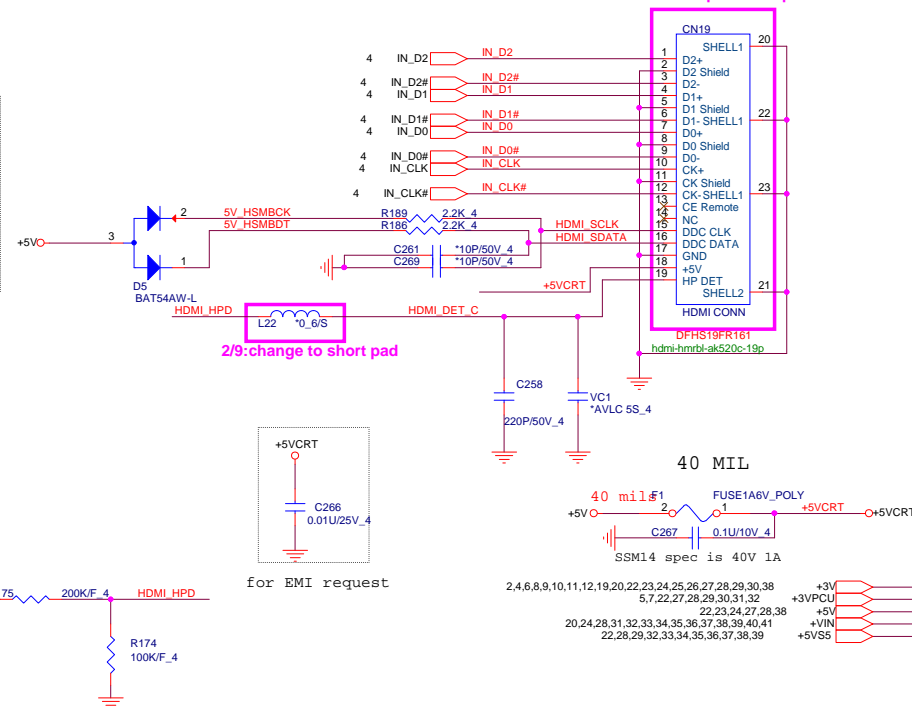


HDMI HPD SENSE

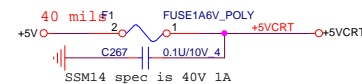


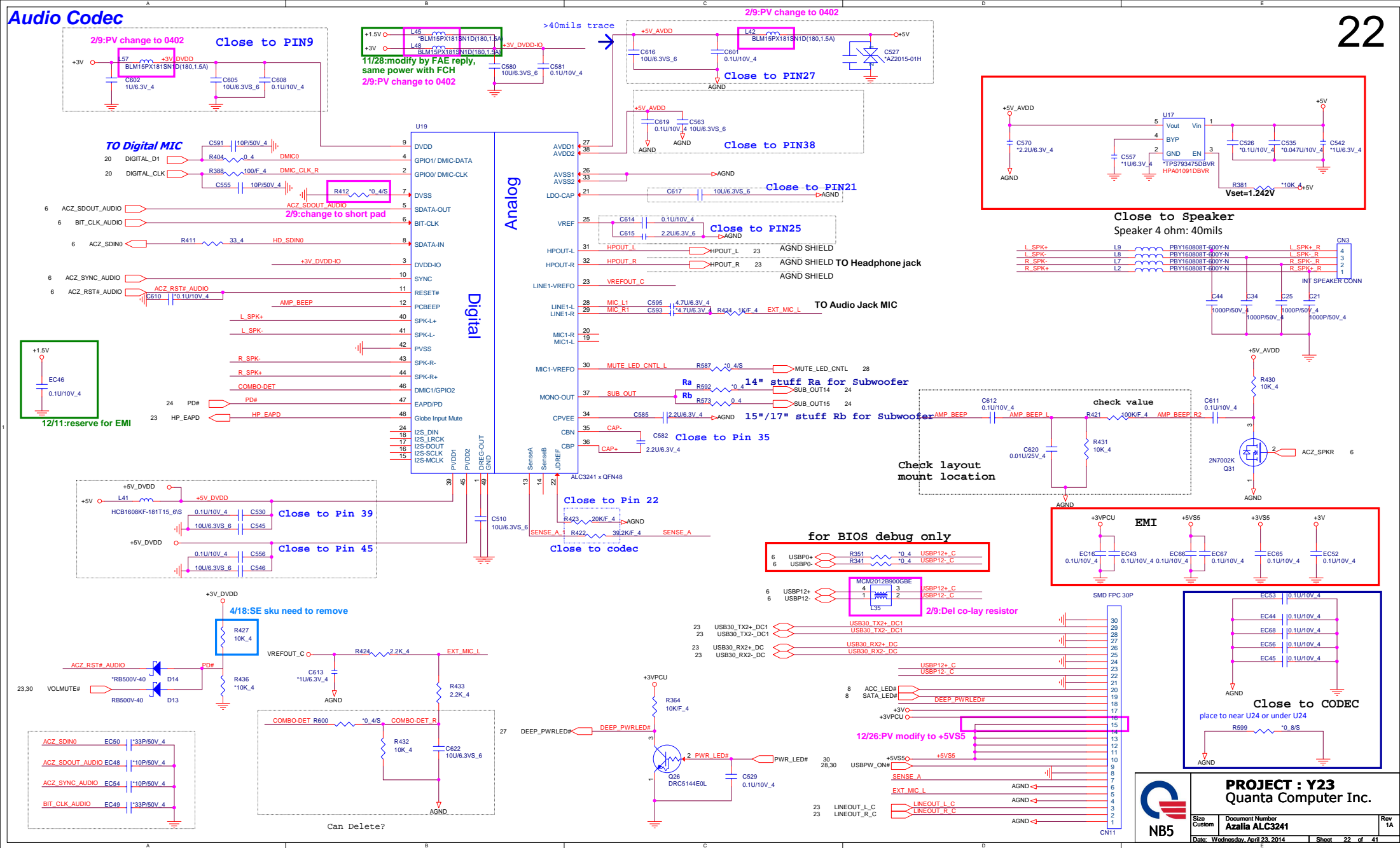
for EMI request

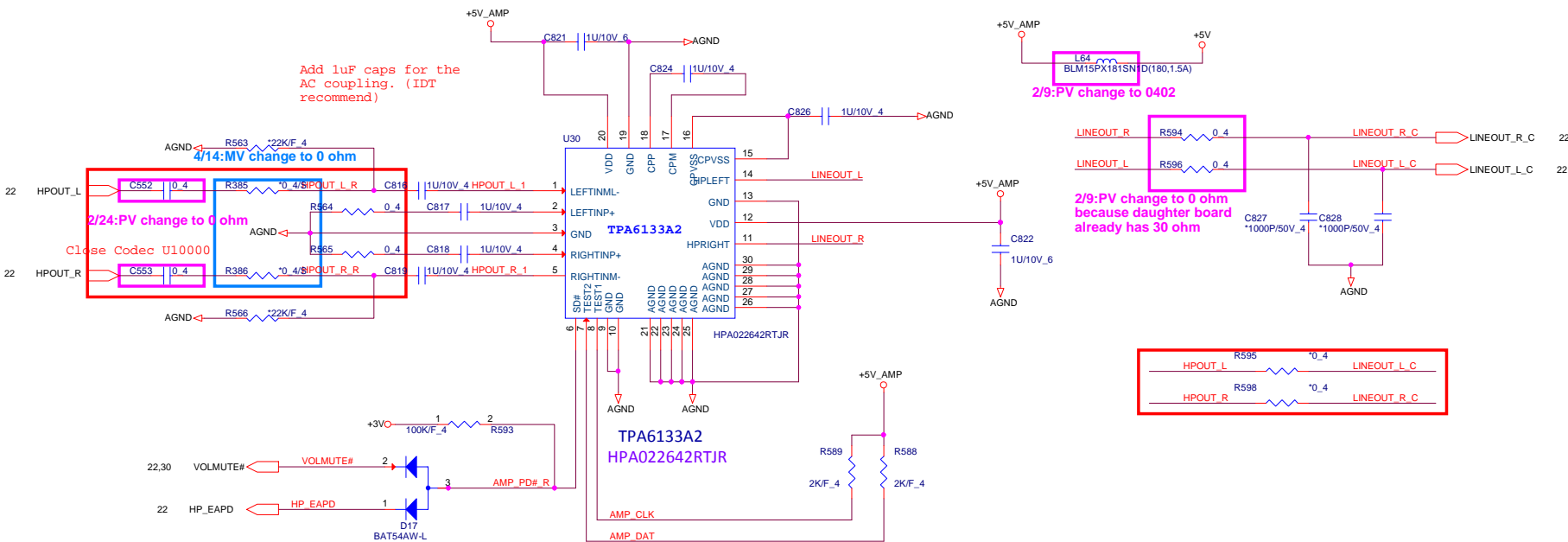
12/26:PV update footprint



40 MIL



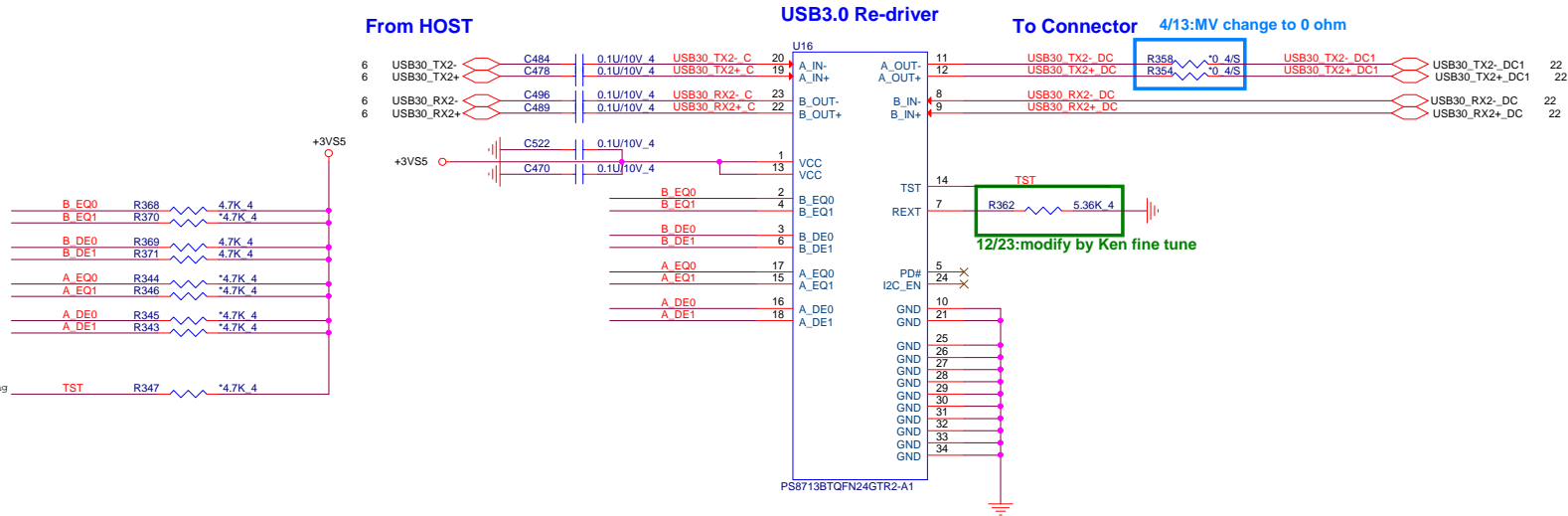




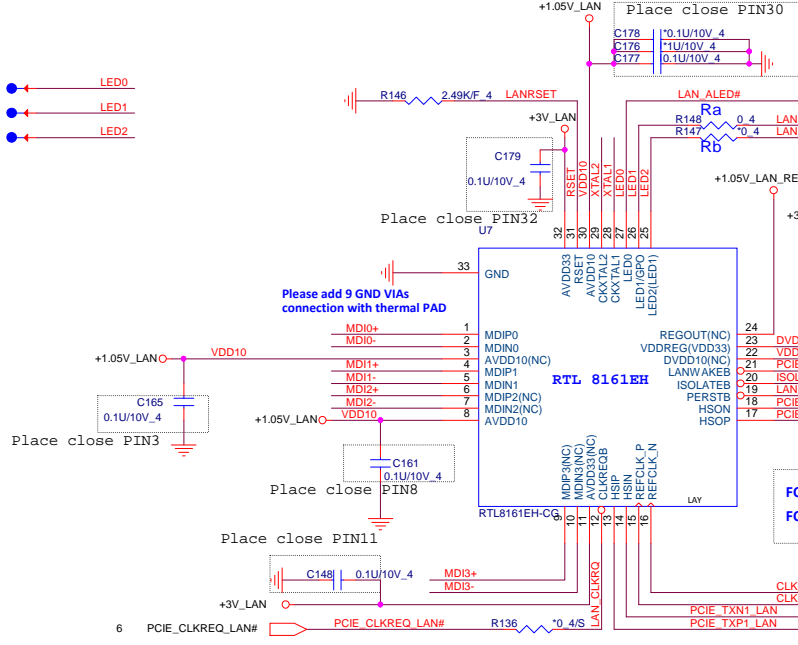
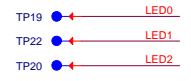
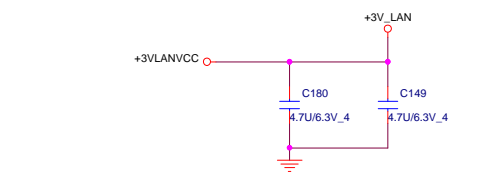
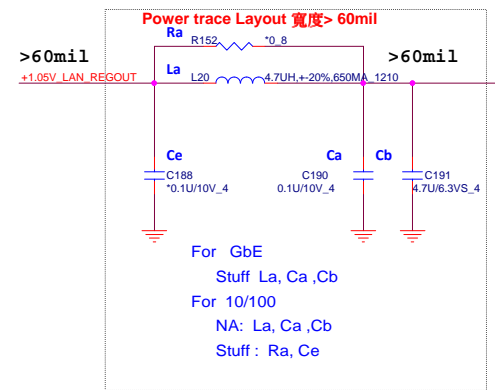
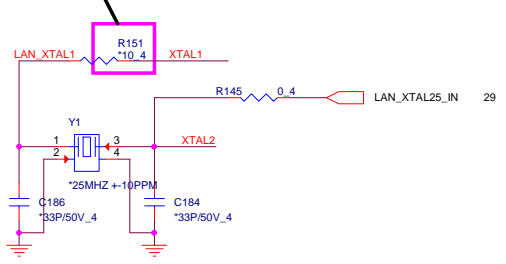
USB3.0 re-driver

A_EQ1	A_EQ0		A_DE1	A_DE0	
B_EQ1	B_EQ0		B_DE1	B_DE0	
0	0	9.5dB	0	0	3.5dB
0	1	13dB	0	1	no de-emphasis
1	0	4.5dB	1	0	2.7dB
1	1	7.5dB	1	1	5dB

TST : Low = Normal LFPS swing / Hight =Turn down LFPS swing



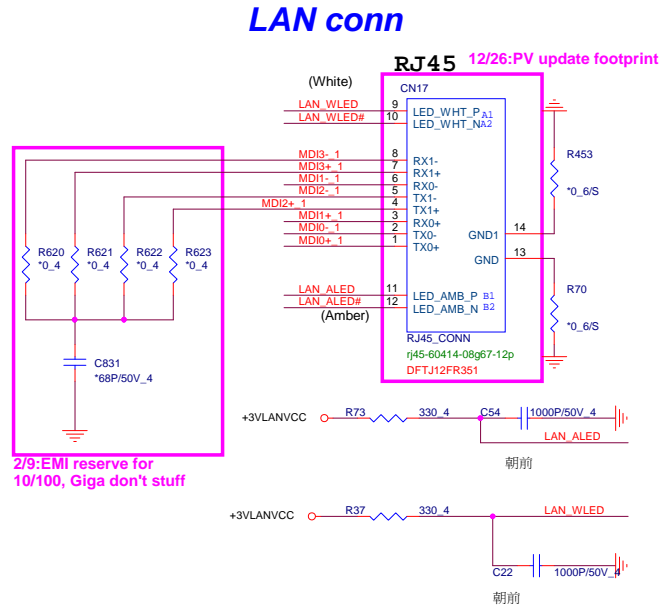
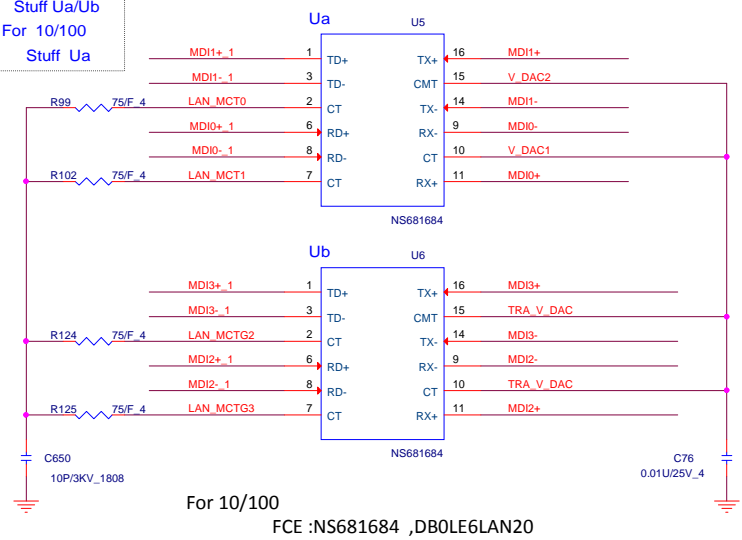
For EMI 0 ~ 22 ohm



For GbE
* Place Ra
For 10/100
* Place Rb

For GbE
* Place C166/C168
For 10/100
* Place C176/C178
12/10:for FAE review

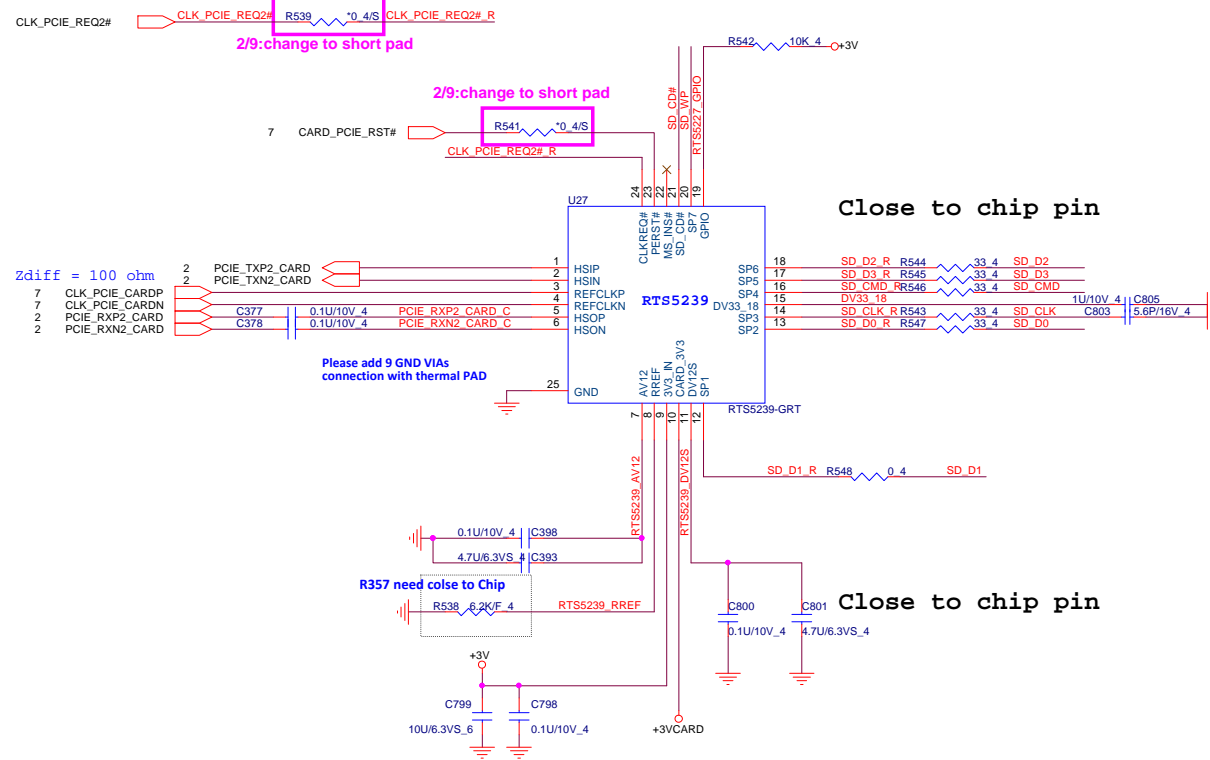
For GbE
Stuff Ua/Ub
For 10/100
Stuff Ua



2,4,6,8,9,10,11,12,19,20,21,22,23,24,26,27,28,29,30,38
29,38
+3V
+3VLANVCC
Place close PIN23 and PIN32

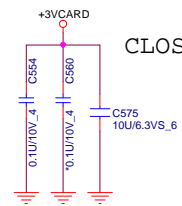
SP1	SD_D1	
SP2	SD_D0	MS_D0
SP3	SD_CLK	MS_D0
SP4	SD_CMD	MS_D2
SP5	SD_D3	MS_D3
SP6	SD_D2	MS_CLK
SP7	SD_WP	MS_BS

Share Pin

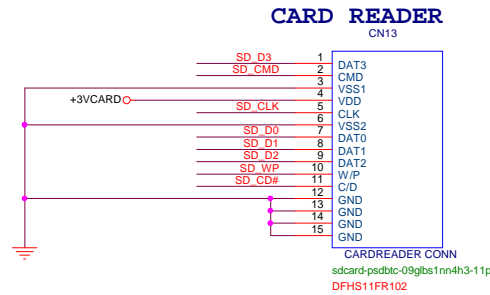
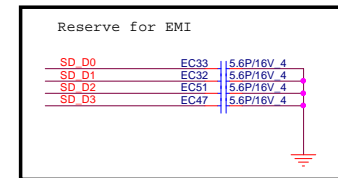


Close to chip pin

Close to chip pin



CLOSE CONN

Change footprint to
sdcard-psdbtc-09g1bs1nn4h3-11p

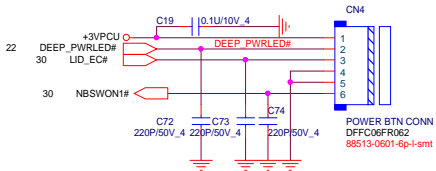
Reserve for EMI



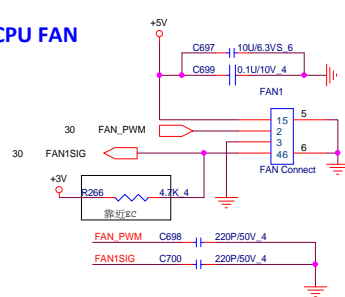
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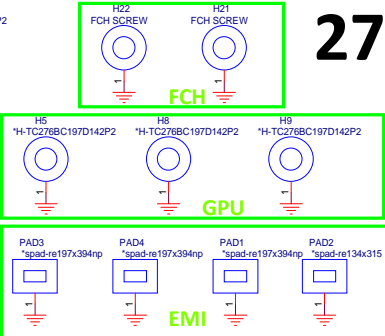
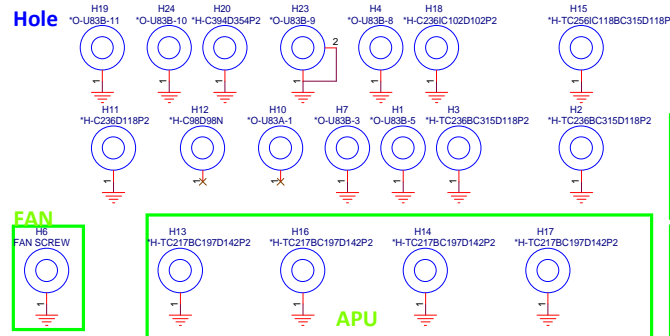
Power Button Connector



CPU FAN

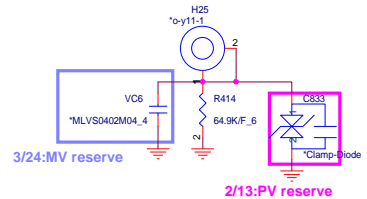
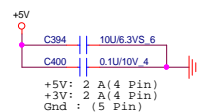
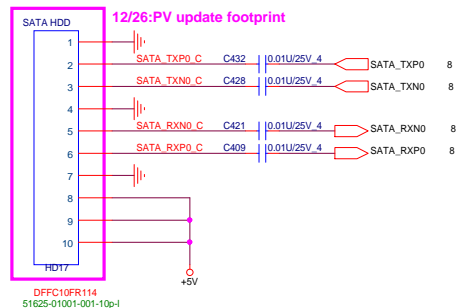


Hole

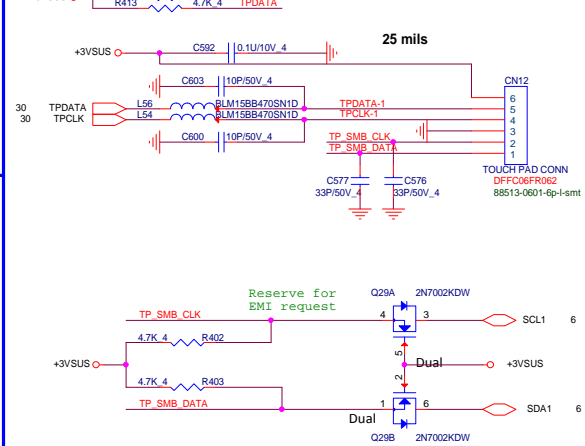


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SATA HDD Connector(Cable type)

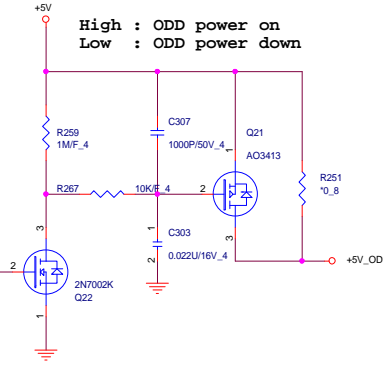
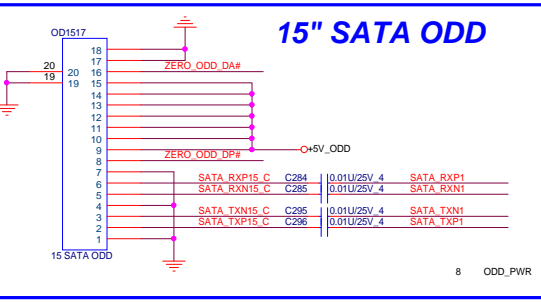
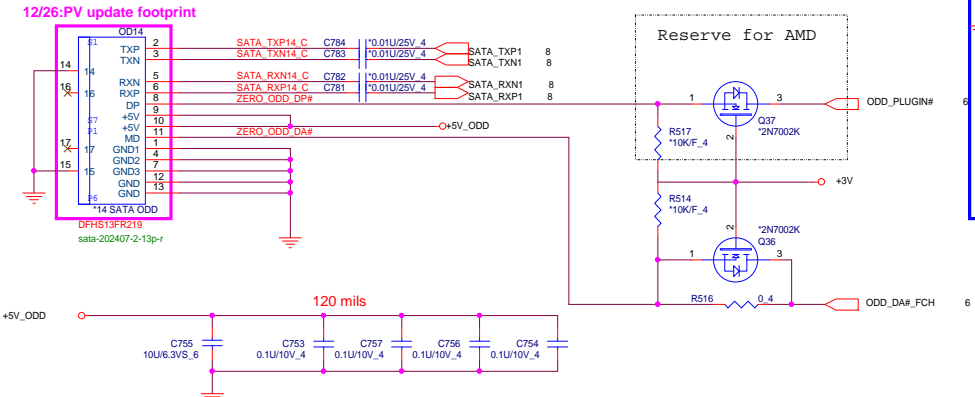


Touch Pad

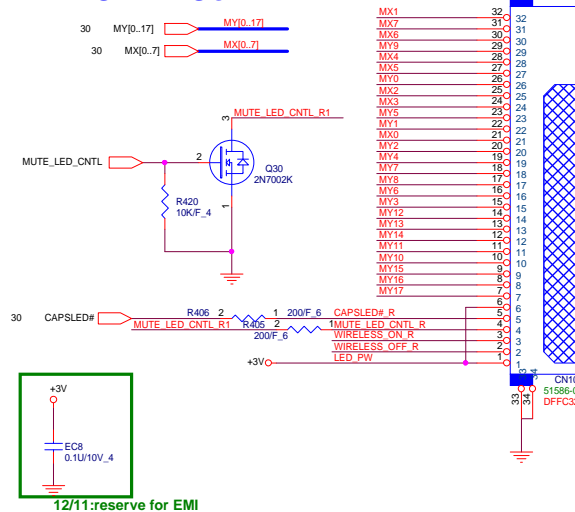


SATA ODD CONNECTOR

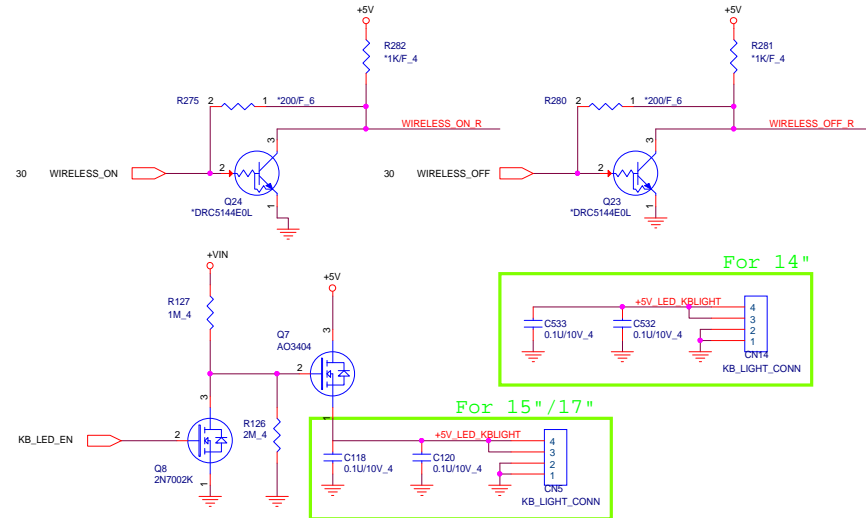
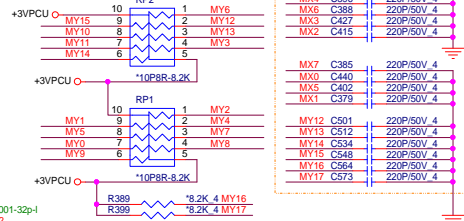
NEW Type Bypass CAP close conn



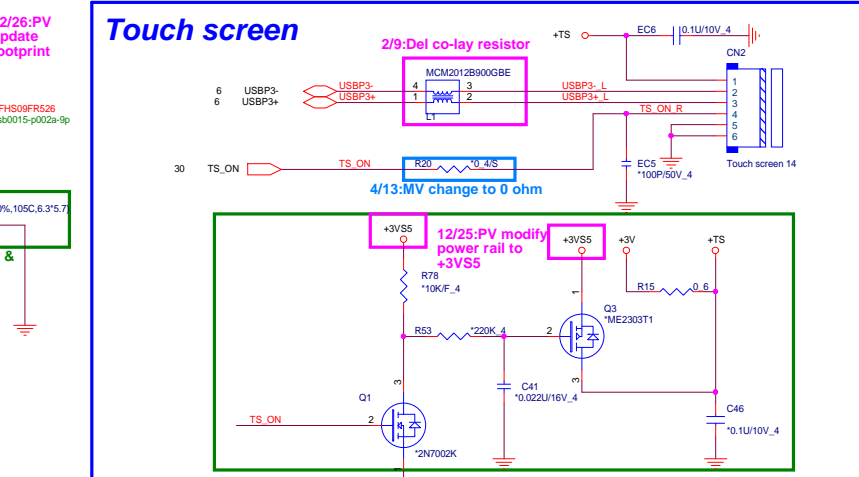
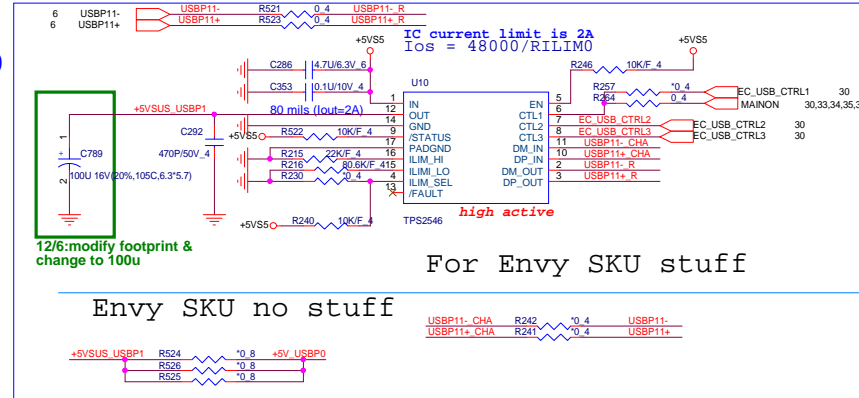
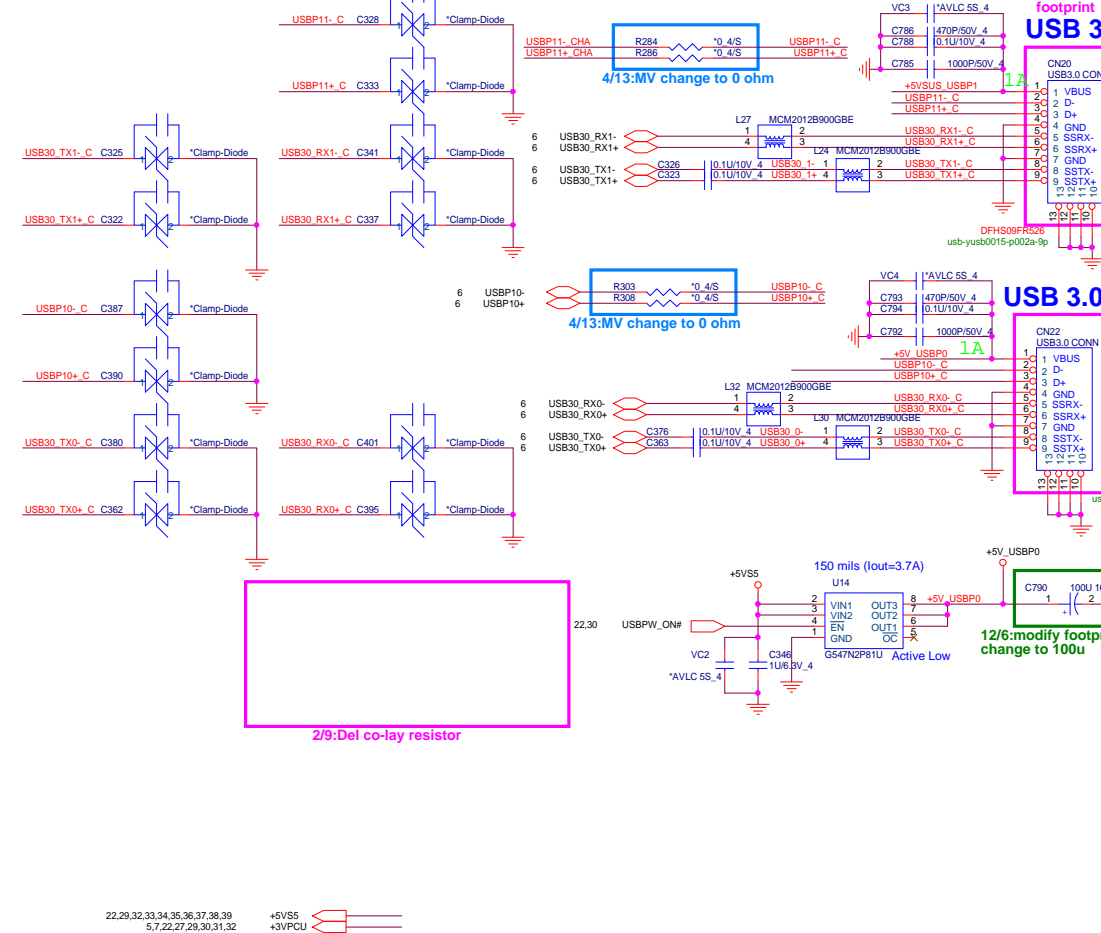
KEYBOARD Con.

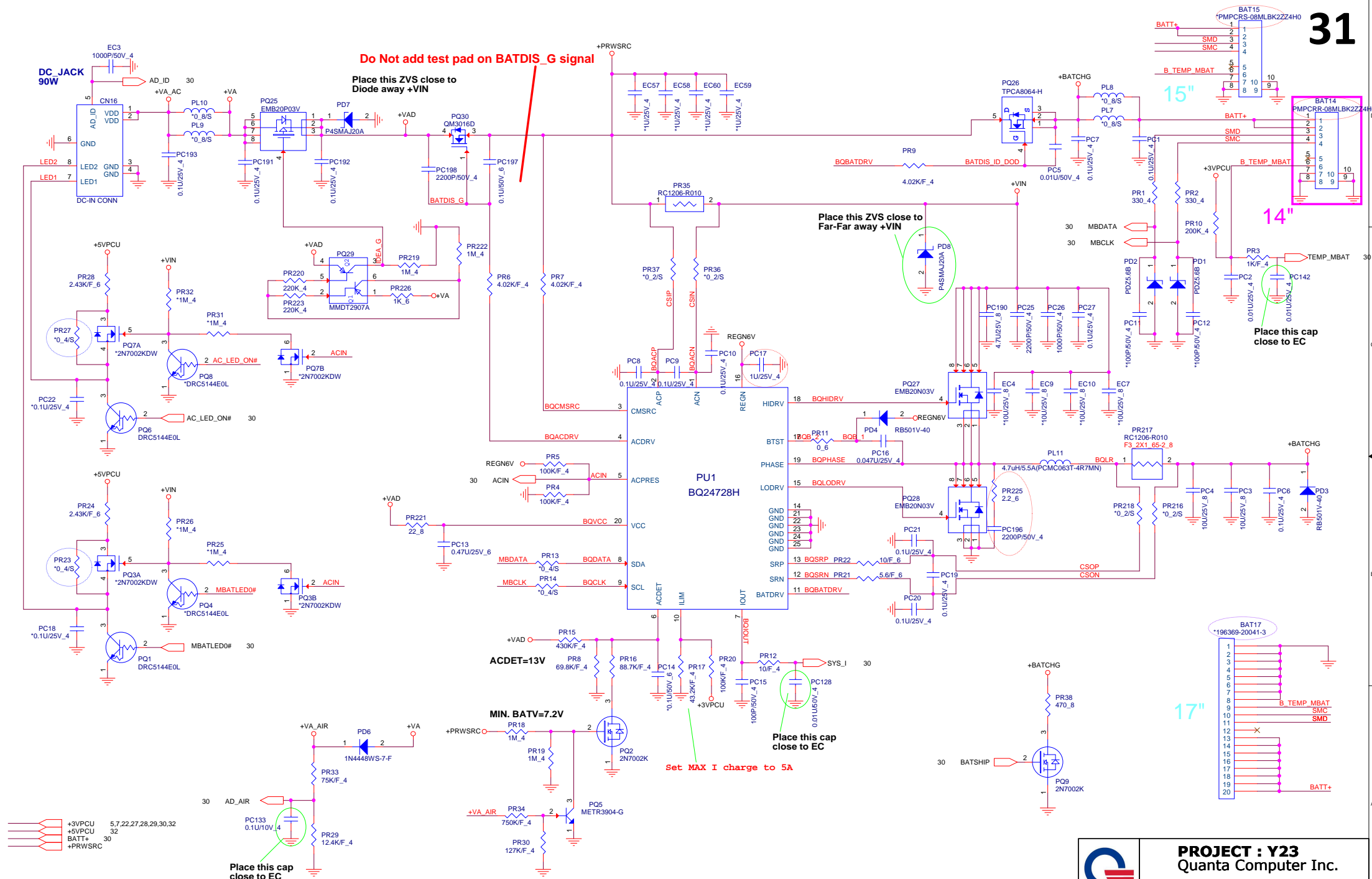


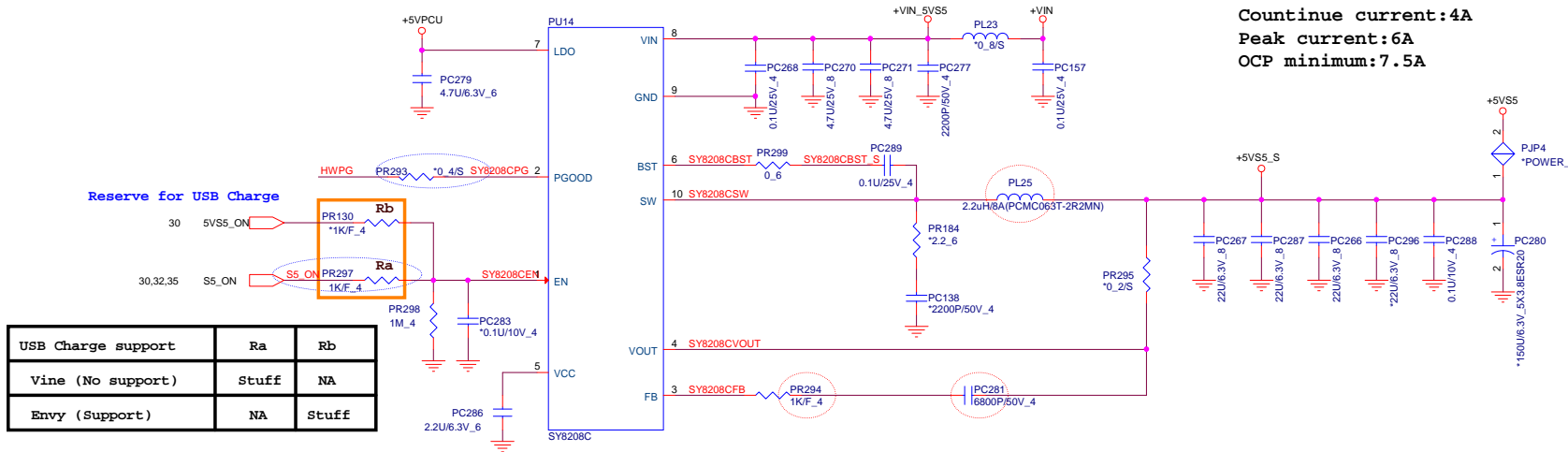
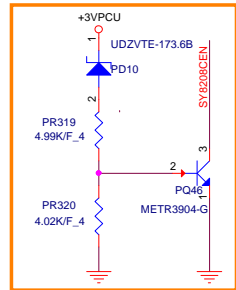
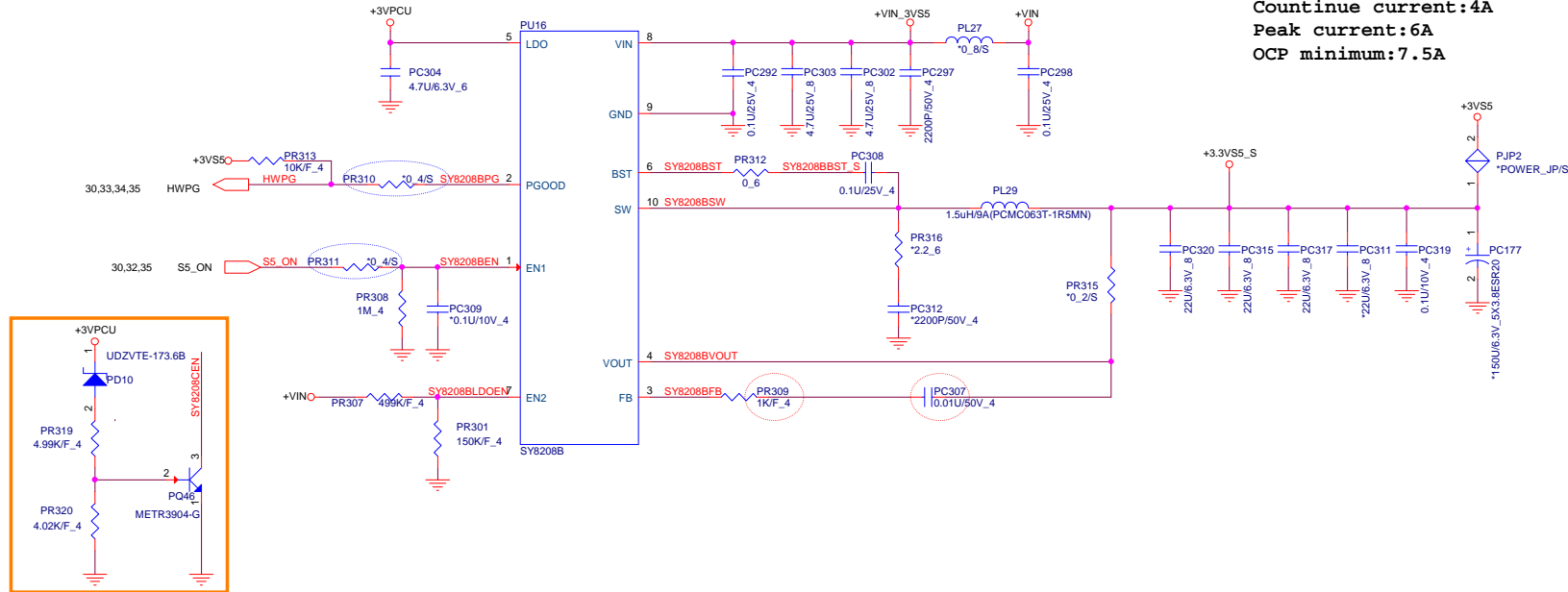
KEYBOARD PULL-UP



USB 2.0/3.0 Combo

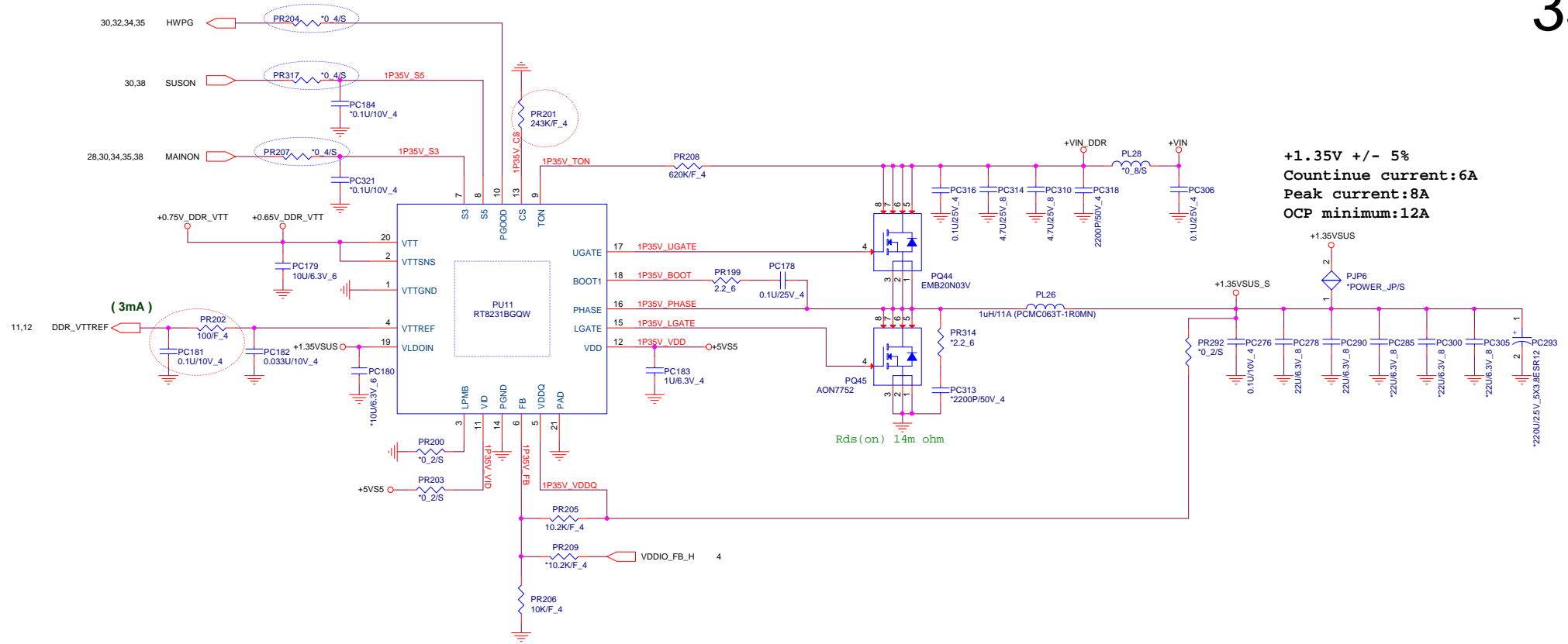






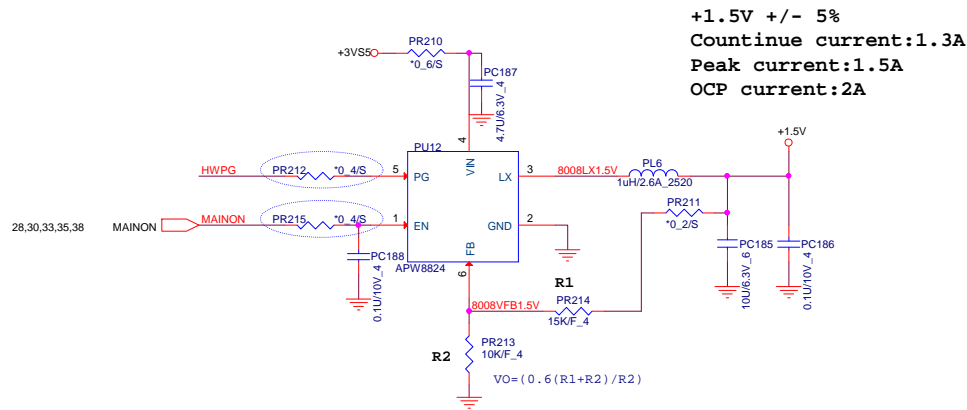
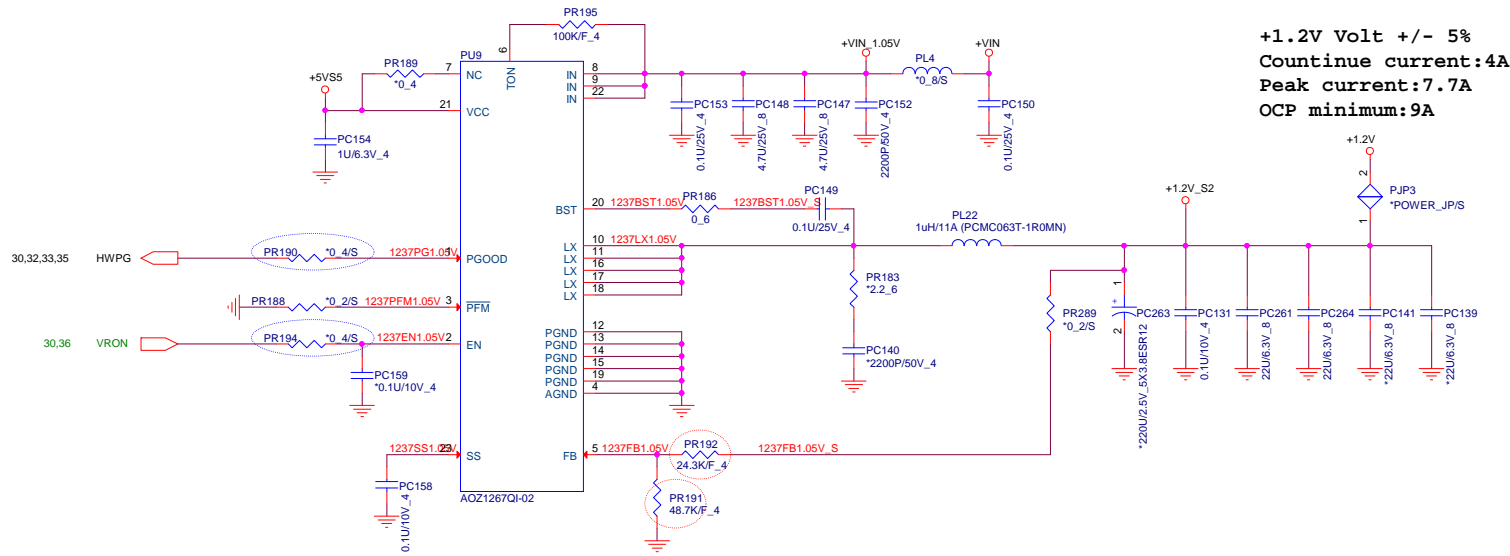
Reserve for USB Charge

USB Charge support	Ra	Rb
Vine (No support)	Stuff	NA
Envy (Support)	NA	Stuff

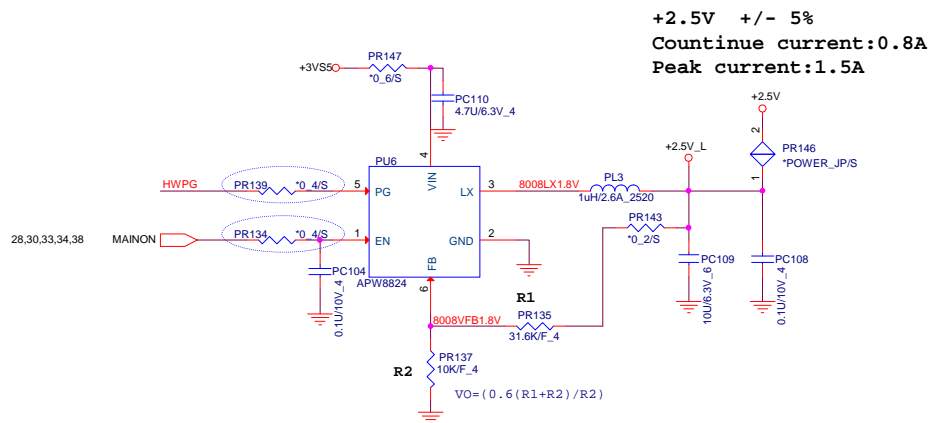
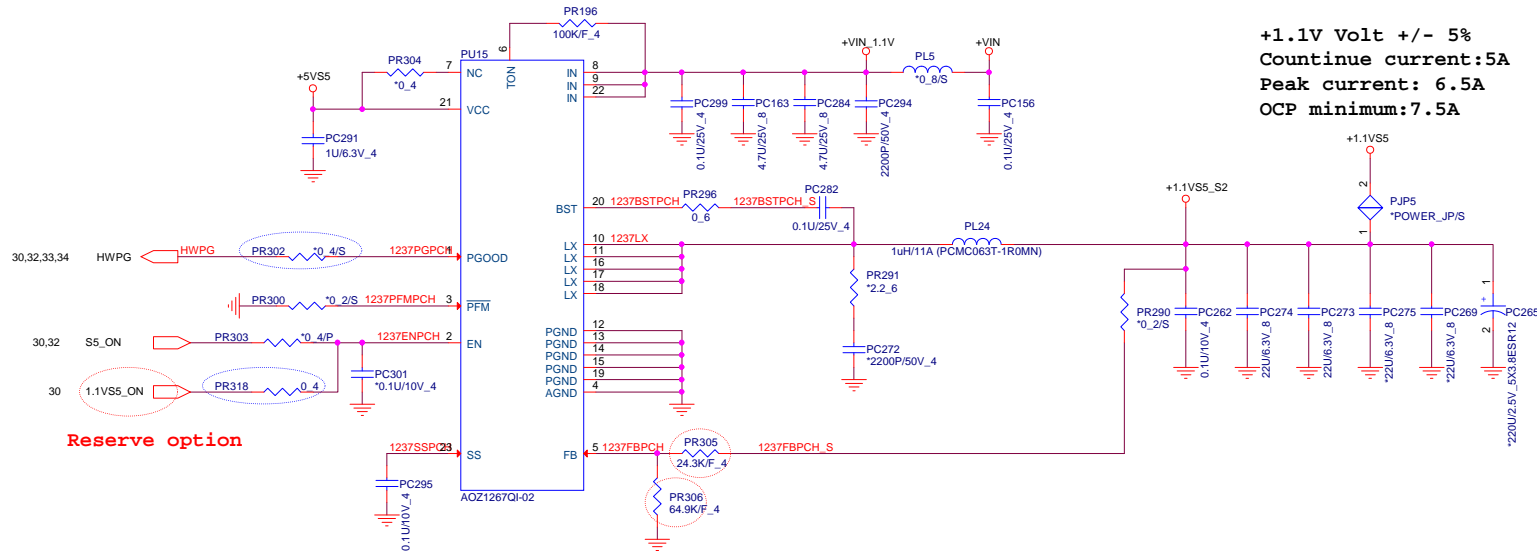


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+VIN	20,24,28,31,32,33,35,36,37,38,39,40,41
+3VSS	6,8,9,10,22,23,28,29,30,32,35,36,38,39,41
+5VSS	22,28,29,32,33,35,36,37,38,39
+5VPCU	31,32



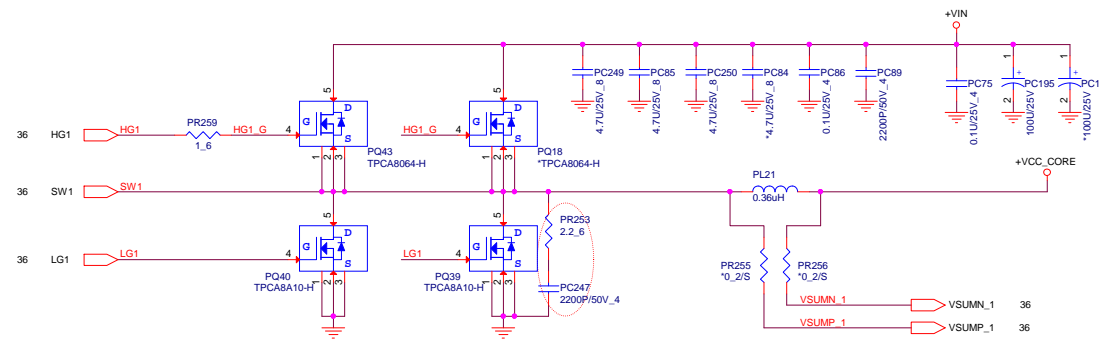
+VIN	20,24,28,31,32,33,34,36,37,38,39,40,41
+3VS5	6,8,9,10,22,23,28,29,30,32,34,36,38,39
+5VS5	22,28,29,32,33,34,36,37,38,39
+1.1VS5	9,38
+5VPCU	31,32



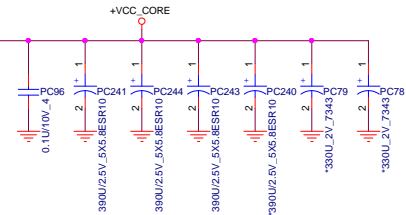
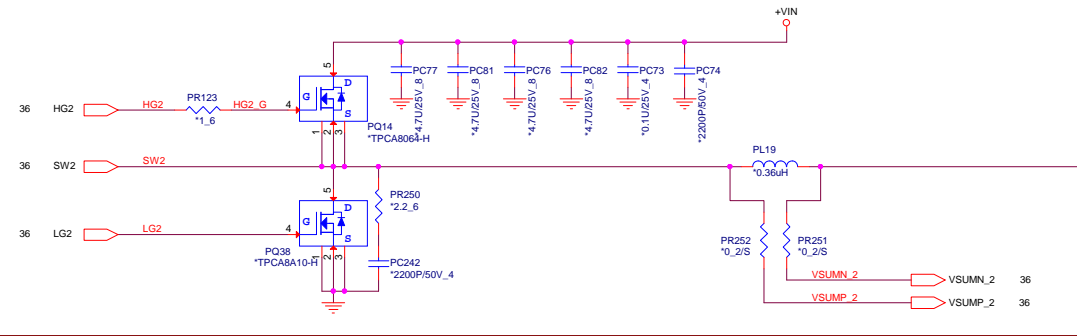
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Size Custom	Document Number +1.1VS5 (AOZ1267)/2.5V	Rev 1A
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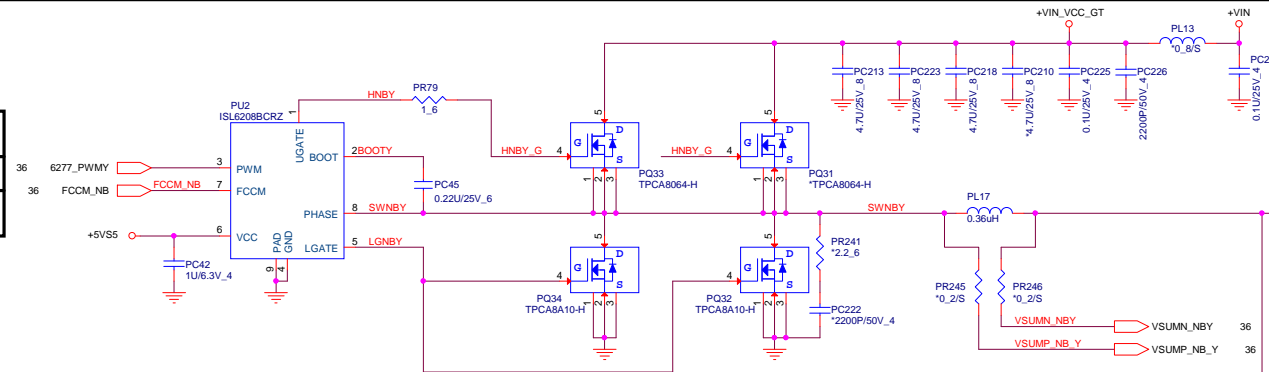
CPU TYPE	MOSFET
25W	1H2L/1phase
19W	1H1L/1phase



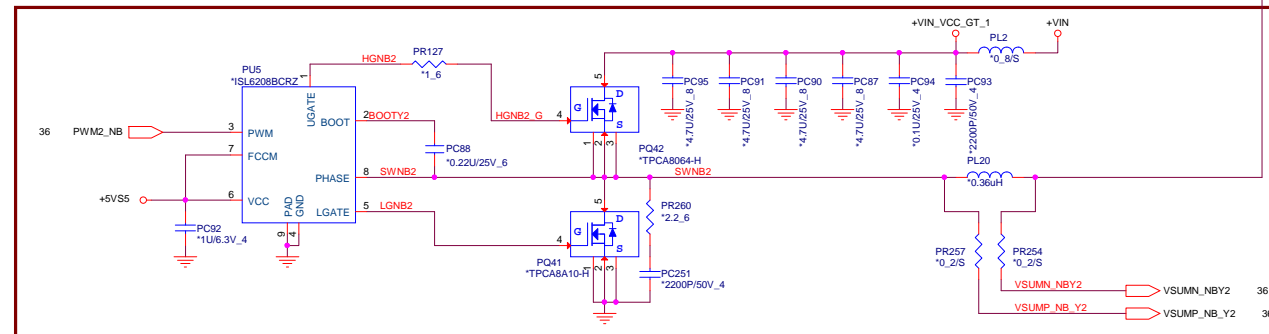
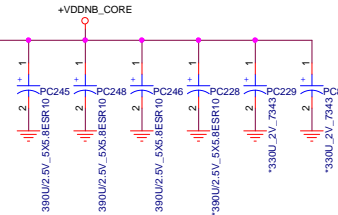
CPU CORE Volt (25W)
Continue current:20A
Peak current:34A
OCP minimum:39A

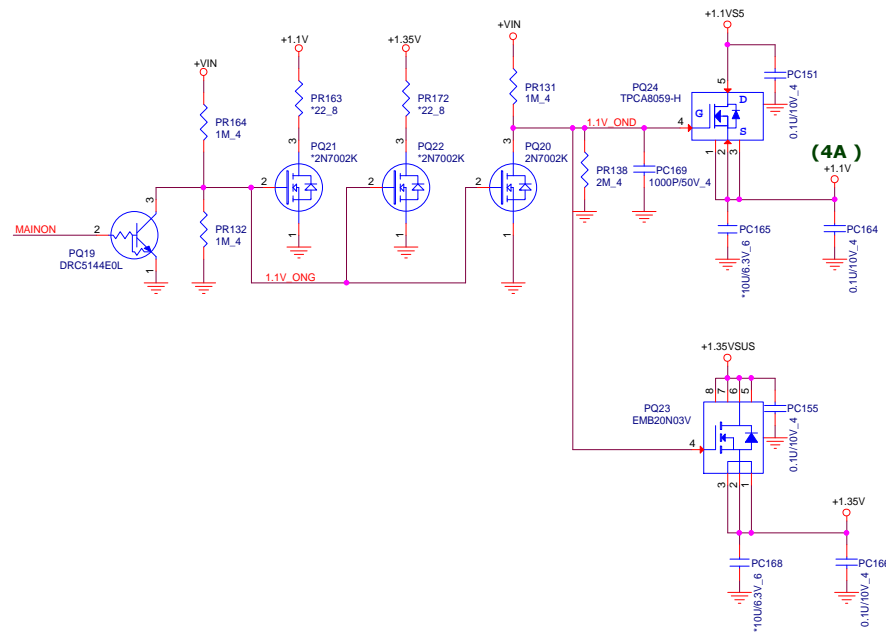
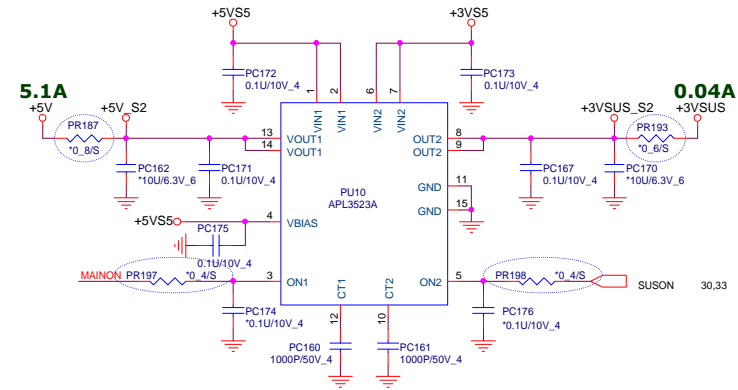
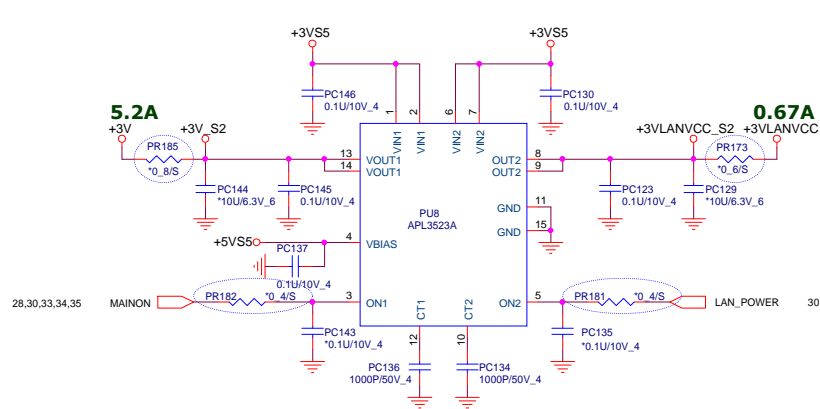


CPU TYPE	MOSFET
25W	1H2L/1phase
19W	1H1L/1phase



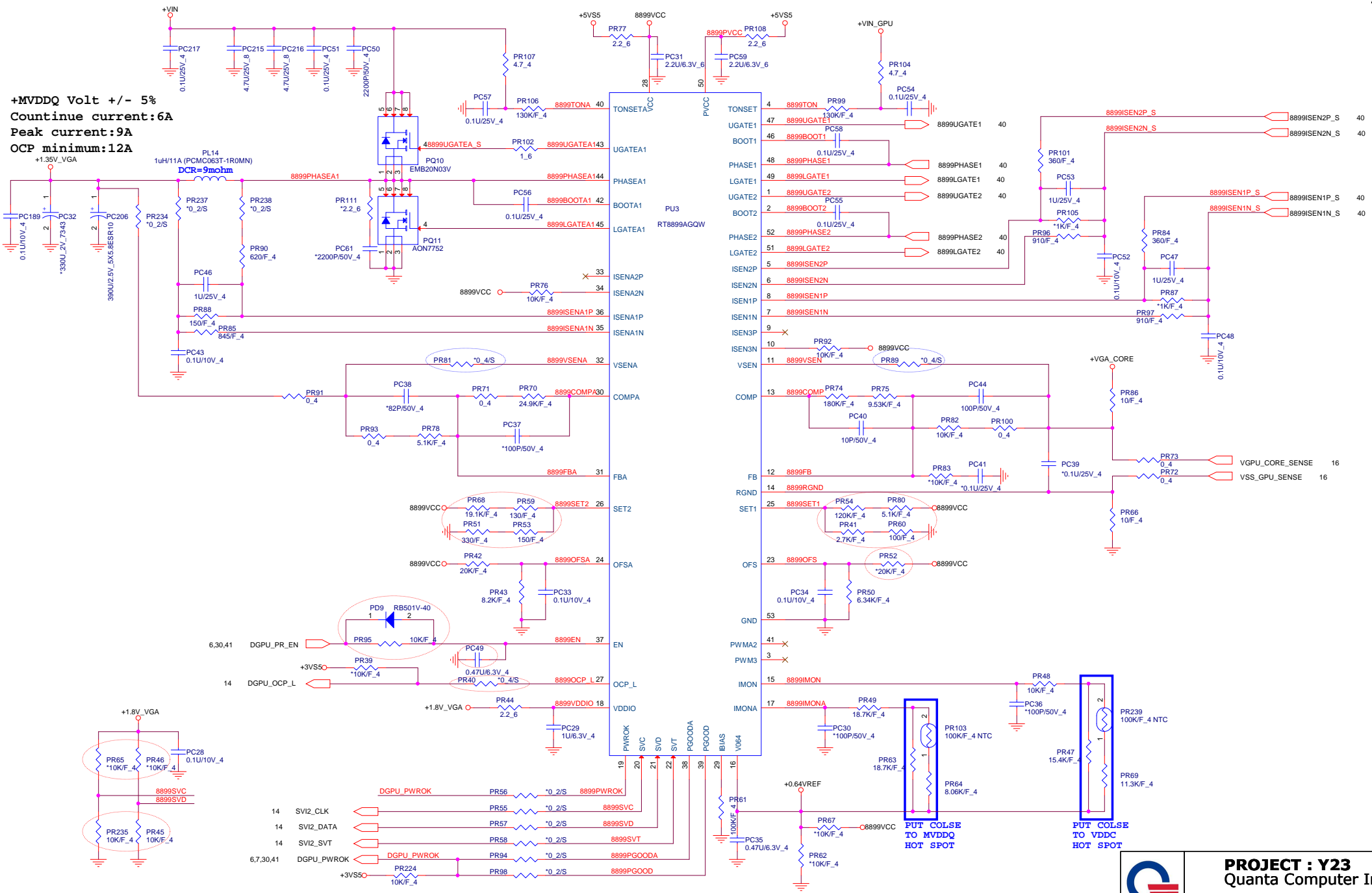
VDDNB Volt
Continue current:14.1A
Peak current:24.1A
OCP minimum:37A

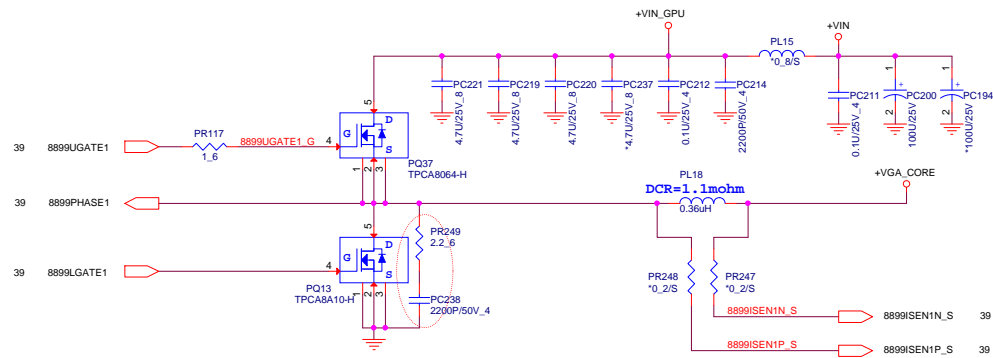




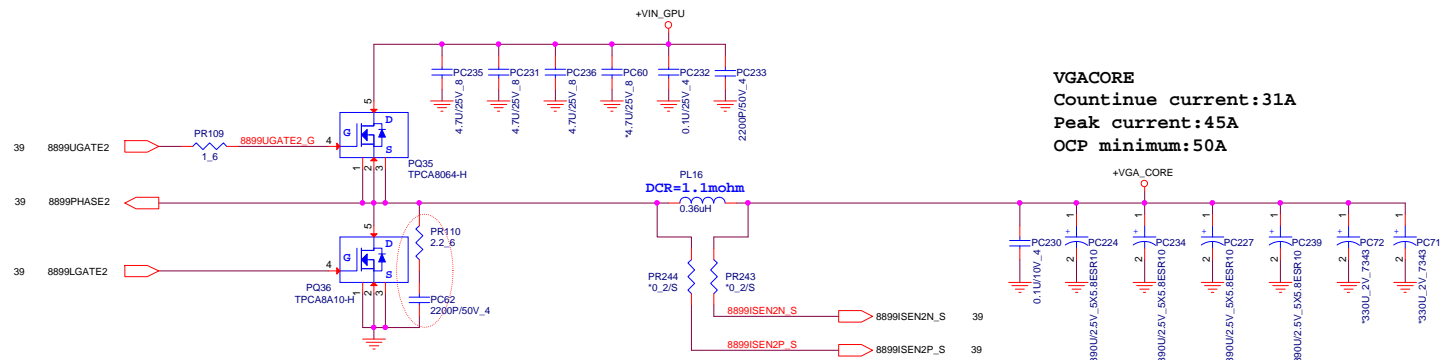
2,4,6,8,9,10,11,12,19,20,21,22,23,24,25,26,27,28,29,30	+3V
21,22,23,24,27,28	+5V
20,24,28,31,32,33,34,35,36,37,39,40,41	+VIN
6,8,9,10,22,23,28,29,30,32,34,35,36,39,41	+3VS5
22,28,29,32,33,34,35,36,37,39	+5VS5
25,29	+3VLAVCC

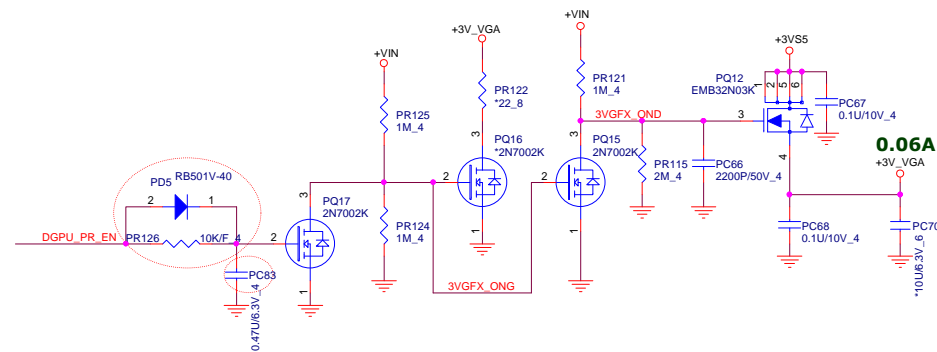
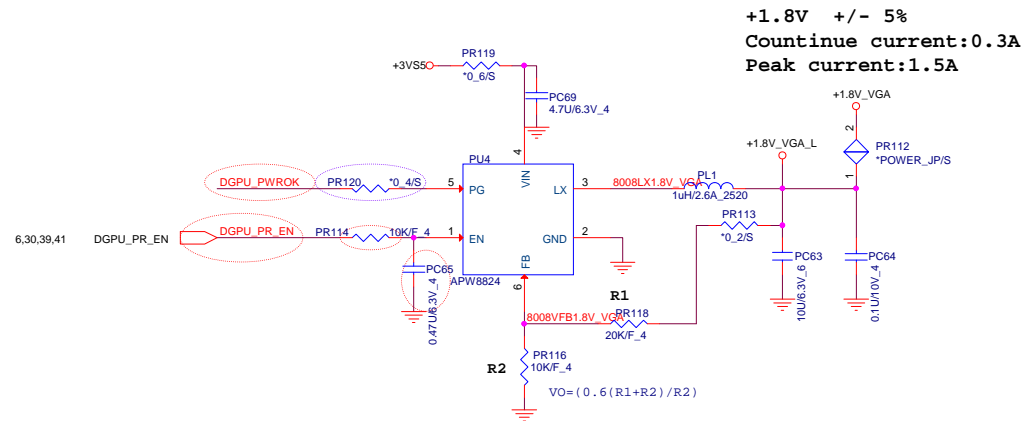
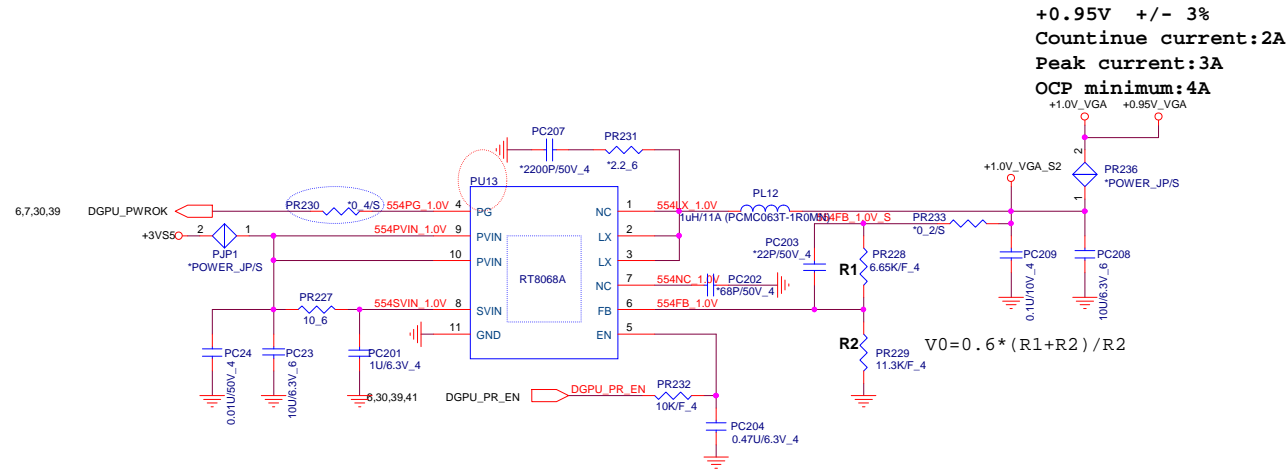
+MVDDQ Volt +/- 5%
Countinue current:6A
Peak current:9A
OCP minimum:12A





VGACORE
 Countinue current:31A
 Peak current:45A
 OCP minimum:50A





+3V_VGA 13,14,16,30
+1.0V_VGA 13,16
+1.8V_VGA 13,14,16,29,39



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